Chip Scale® REVIEW

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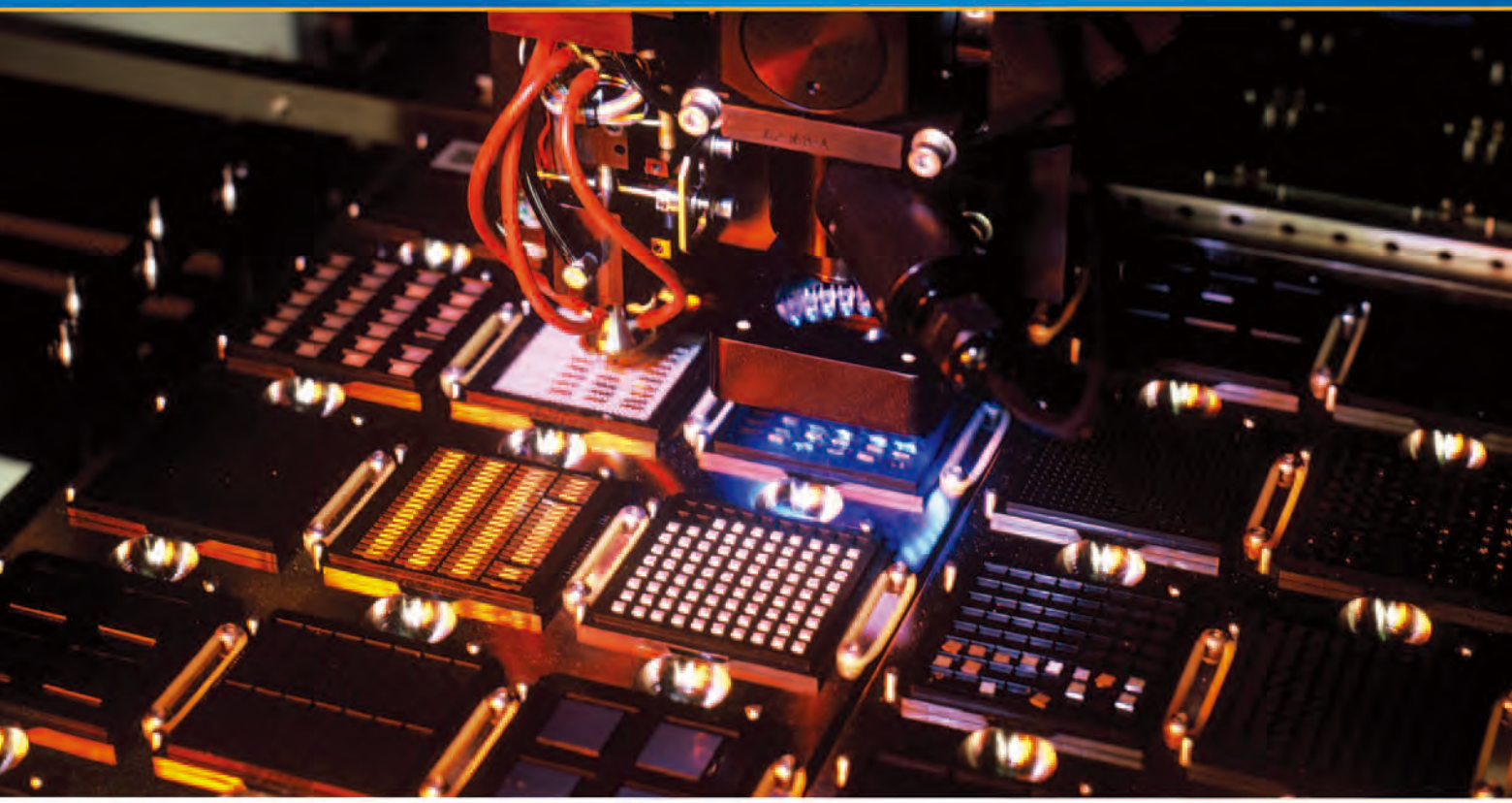
The International Magazine for the Semiconductor Packaging Industry

Volume 15, Number 6

November December 2011

- Dicing 101: LEDS, Laser, MEMS
- Trends Driving WLP and 3D
- Direct Copper Bonding for High Density Applications
- Electroless Plating for Improved Test
- Solder in the Age of 3D
- International Directory of Solder and Flux Suppliers



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CONTENTS

November December 2011
Volume 15, Number 6

In the midst of tremendous technological changes in manufacturing methods, semiconductor assembly and test houses are still relying on known and reliable processes. Solders and fluxes have evolved into new forms, but the principle of forming electrical interconnects from a self-leveling, molten solder joint cleaned by an appropriate semiconductor grade flux remains a core element of the assembly process. Front cover image courtesy of Indium Corporation.

Chip Scale REVIEW™

The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

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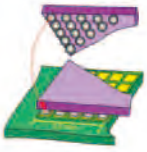

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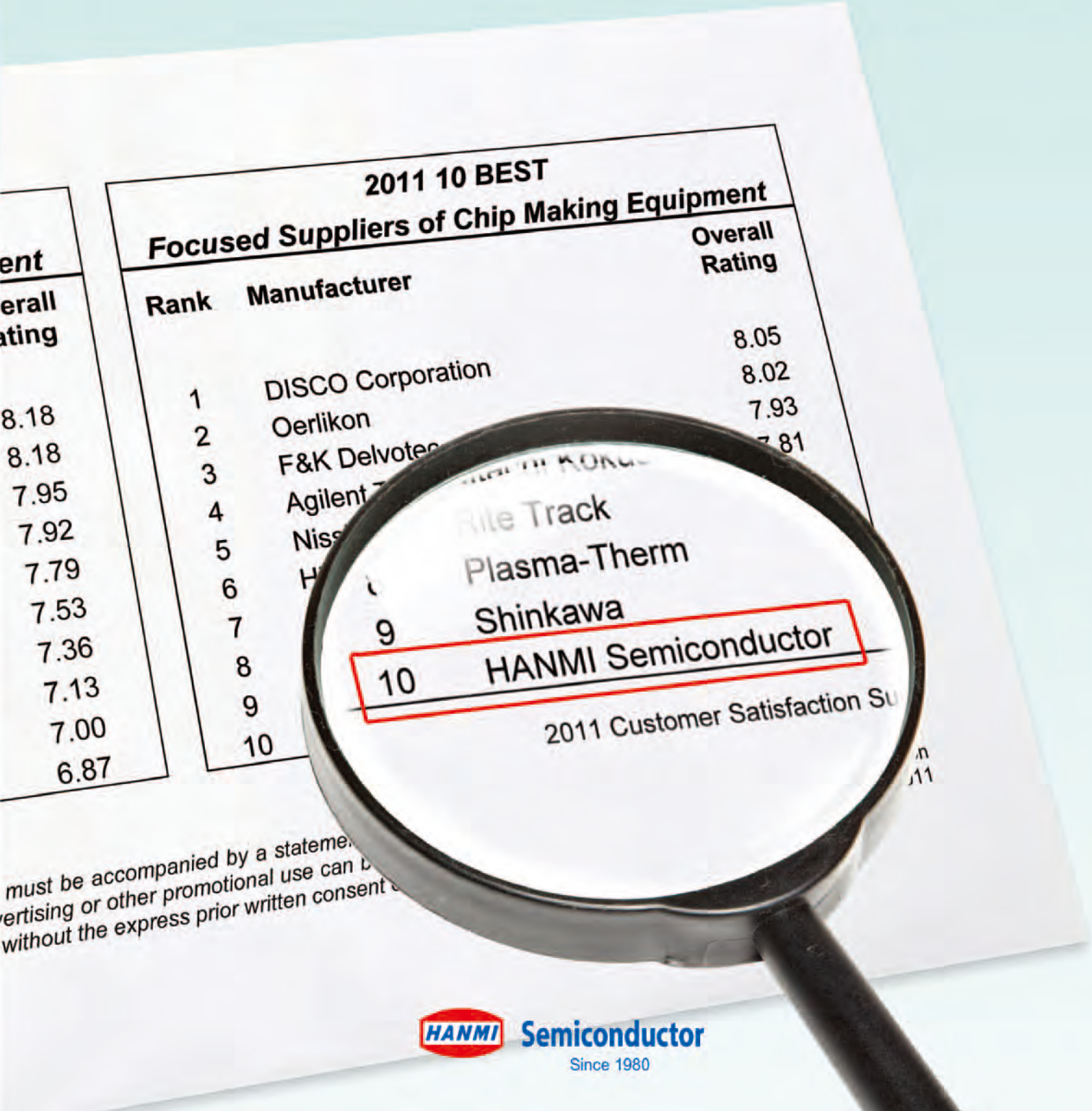

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CONTENTS

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FROM THE PUBLISHER

2011 in Retrospect

The past 12 months have been a busy time for everyone at *Chip Scale Review*. As this is our last issue of 2011, it seems to be a good time to reflect on our progress and look forward to what 2012 will bring for us and for the industry at large.

2011 brought many things to the table for us all. Once again, we successfully published six spectacular issues of *Chip Scale Review* in both print and digital covering technology advancements in established semiconductor packaging processes and technologies, as well as a myriad of innovations being pursued by research institutes all over the world (SEMATECH, Ga Tech, ITRI, and CEA Leti). Additionally, our eNL *CSR Tech Monthly*, still in its infancy, has gained momentum as a supporting media buy to the print for CSRs advertisers. 12 issues of the *CSR Tech Monthly* were broadcast in 2011 with another 12 on the way in 2012. I'm happy to report that the 2012 media kit is hot off the press and available online.

Chip Scale Review supported three major trade events in 2011 as the Official Media Sponsor for both the BiTS Workshop and the Electronic Components Technology Conference (ECTC); as well as our very own co-sponsored event with SMTA – the International Wafer-Level Packaging Conference (IWLPC). You can read up on this year's IWLPC in the Industry News section of this issue (pp. 12-13) or check out the video clips on the CSR website.

Also vital to the success of *Chip Scale Review* our editorial advisors, who help navigate the editorial direction and scope of the magazine and assist in recruiting exclusive technical features throughout the year. On behalf of everyone at CSR, we continue to appreciate those members who have been long standing advisors over the years including: Tom Di Stefano of Centipede Systems; Andy Mackie of Indium Corporation; CP Wong, Regents Professor at Georgia Institute of Technology; Guna Selvaduray, Professor Materials Engineering at San Jose State University; Ephraim Suhir of ERS Company; and Nick Leonardi of Premier Semiconductor. Newcomers to this distinguished list include: Rolf Aschenbrenner, Deputy Head at Fraunhofer Institute; Alissa Fitzgerald of AM Fitzgerald & Associates; Joseph Fjelstad, Verdant Electronics; Scott Jewler of Powertech Technology Inc; John Lau of ITRI; Venky Sundaram of 3D PRC, Georgia Institute of Technology; and Fred Taber Chairman of the BiTS Workshop.

Chip Scale Review's past and future success can be attributed to the editors and contributors of the columns, the guest editorials and of course the technical features. I would like to personally thank and acknowledge each and every columnist and author who contributed their article to CSR. A special thank you to Technical Editor Ron Edgar who supported CSR throughout the year and has provided his final column in this edition entitled "Act IV". After deliberation Ron has decided to focus on his career at hand. We wish him well and the very best ahead.

Kim Newman
Publisher

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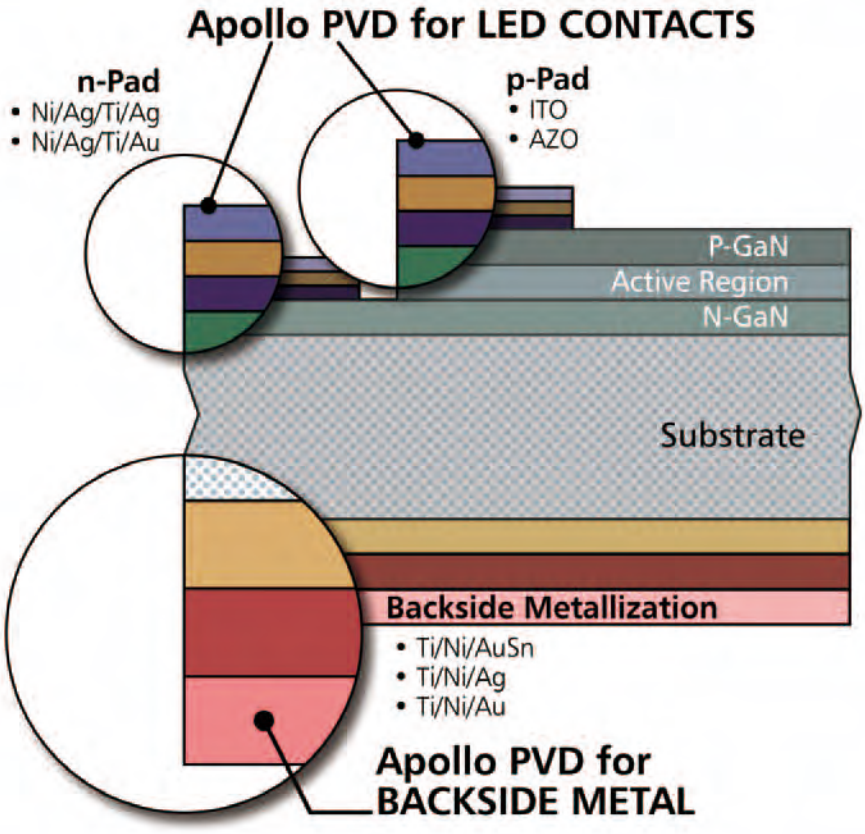
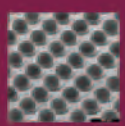
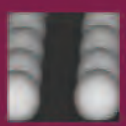



Lead Free


RDL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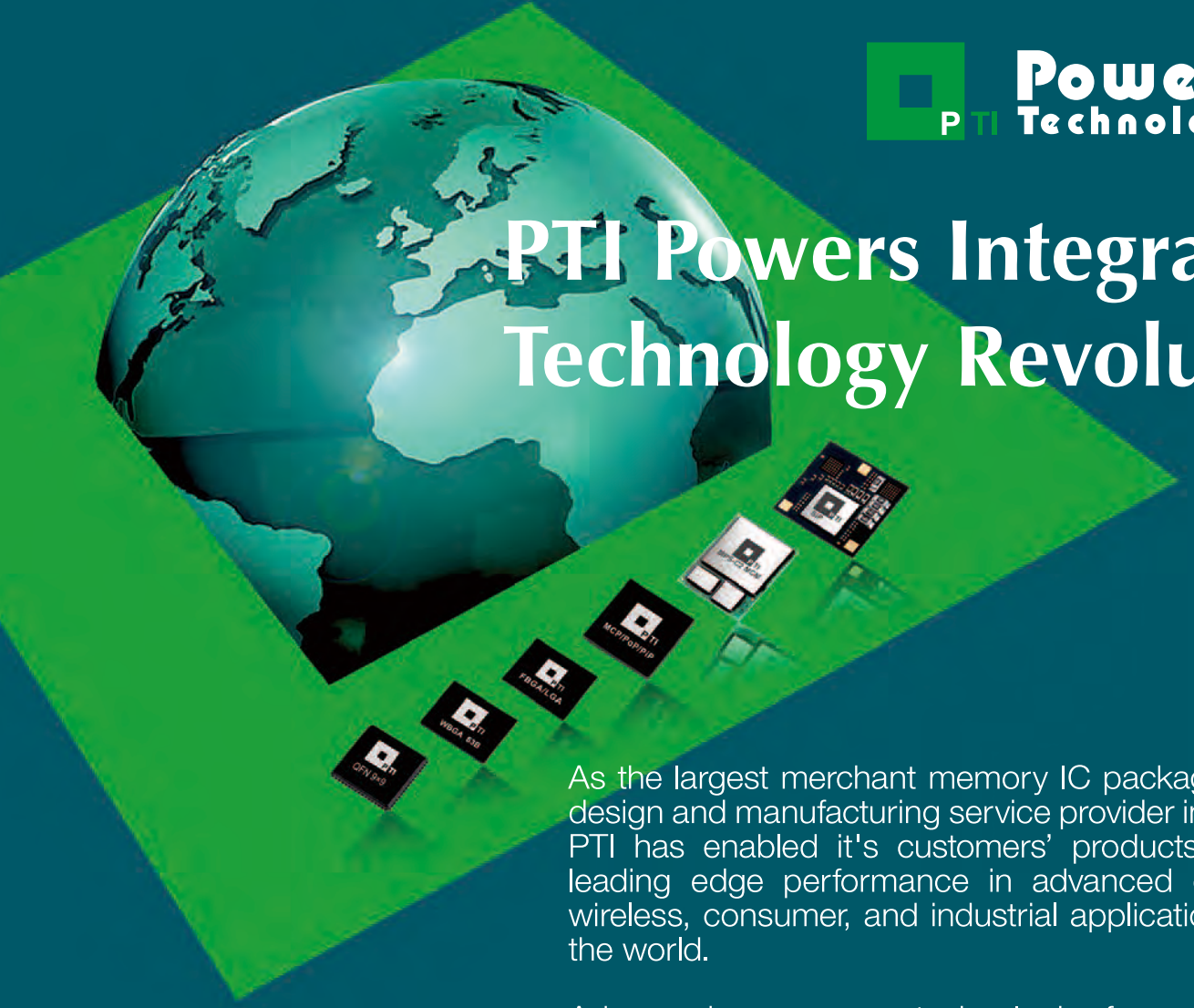

As the largest merchant memory IC package and test design and manufacturing service provider in the world, PTI has enabled it's customers' products to deliver leading edge performance in advanced computing, wireless, consumer, and industrial applications around the world.

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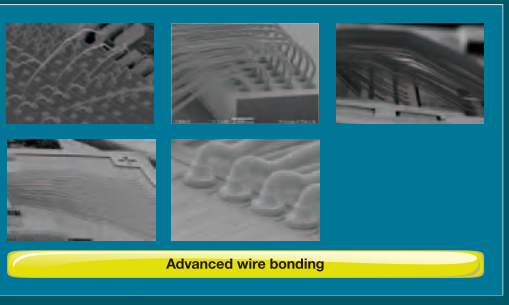
With a focus on delivering the next generation of IC integration solutions, PTI will leverage these core strengths to bring advanced 3D IC solutions incorporating TSV (through silicon via) technology to market.

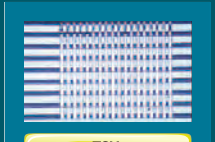
wafer thin to 20um

High density chip stacking



Advanced wire bonding

Cu pillar bump



TSV

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Changes to Patent Legislation

By Jason Mirabito, [Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C.]

On September 16, 2011, President Obama signed the Leahy-Smith America Invents Act, probably the most comprehensive patent reform legislation in the last 40 years. This article focuses on two changes that have great impact. The first is a fundamental change to the U.S. patent application filing system and the second is a fundamental change to the ability of third parties to challenge patents.

First-to-File System Enacted

For many years under U.S. Patent Law, the U.S .has been under a "first to invent" system. According to this system, even if there are two (or more) persons file for a patent at the United States Patent Office (USPTO), the earliest of those two inventors is not necessarily considered to be the inventor. In what is called an interference proceeding, the USPTO determines the first inventor by looking at invention records, etc. These interference proceedings are long and have been traditionally very expensive. The U.S. has now gone to a first- to-file system.This means simply, whoever gets to the USPTO first and files their application first is the first inventor. Period. It is believed that this change puts the U.S. in the same position as every other country in the world, which all have first-to-file systems. During the pendency of this portion of legislation, there was much criticism of this shift to a first-to-file system by small inventors and some small companies, who argue that this change would benefit larger companies that have the money and wherewithal to file applications early. Time will only tell whether this becomes an impediment for small companies to file patent applications.

Enacting Post Grant Procedures

There have been allegations that the USPTO allowed patents to issue that should not have issued in the first place. Therefore, Congress decided that there were not sufficient safeguards built into the USPTO system to catch "bad" patents. Since at least 1980, parties have been able to file requests for reexamination. This part of the pre-existing patent statute allows third parties (even the patent owner) to present the Patent Office with prior art consisting of printed publications and allege that the claims as issued in the patent are not valid on the basis of this same prior art. Up until recently, the only type of reexamination that was permitted was a so called Ex Parte Reexamination, where the party requesting the reexamination (the requestor) had very limited participation. Circa 1999, the so called interpartes reexamination system came into being that allowed requestors relatively full participation in the reexamination process, including the ability to appeal through to the U.S. Court of Appeals for the Federal Circuit.

The just enacted law now provides four avenues by which requestors can challenge the validity of the claims of a patent. The first is the so-called Post Grant Review, which will allow third parties to challenge the validity of a patent within nine months of the patent issue date. It is permissible to bring any ground or grounds for invalidity to the attention of the USPTO, not just limited to prior printed applications. The European Patent Office has a similar post-grant review and the change in the U.S. law makes U.S. law conform to that of the European Patent Office.

Under the second procedure, Inter Partes Review, any time after the nine month post-grant period expires, a requestor can request a reexamination of the patent; but here the request is limited to prior printed publications. While the entire provision does not come into effect immediately, the part that relates to the standard under which the USPTO will grant a request for a review comes into effect immediately. The old test was that of "raising a substantial question of patentability". The new test is "whether there is a reasonable likelihood that the petitioner will prevail with respect to at least one challenged claim". This will raise the bar and the level of proof needed before the Patent Office will grant such a petition.

A third addition is called Supplemental Examination, which can be requested by the patent owner only and allows the patent owner to have the USPTO consider information related to the patent.

Fourth, and finally, the "old" ex parte reexamination law will still continue to exist and, in fact, coexist with the other provisions that have been enacted.

It is expected that the new and expanded post grant procedures will keep the USPTO very busy in the coming years.

Backside Illumination Highlights Direct Bonding Technology

By Kathy Cook, [Ziptronix]

With backside illuminated (BSI) sensors in high-volume production and interposers seemingly ready to take off, the time for 3D integration has finally come. Direct bonding has played a key role in enabling BSI image sensor manufacturing and will continue to do so in other 3D applications.With the technology now licensed commercially, there are fewer questions about the feasibility of direct bonding technology than in the recent past.

BSI image sensors have better performance than their FSI counterparts. The improved performance is due to the fact that the metal interconnect layers are positioned below the photodiode layer as opposed to above it (**Figures 1a and b**).

Within the BSI image-sensor manufacturing space, direct bonding technology enables device manufacturers to achieve lower distortion than other technologies (**Figures 2a, b and c**). The result is that pixels can be scaled smaller, resulting in more die per wafer. This in turn produces higher yields and lower cost per die.

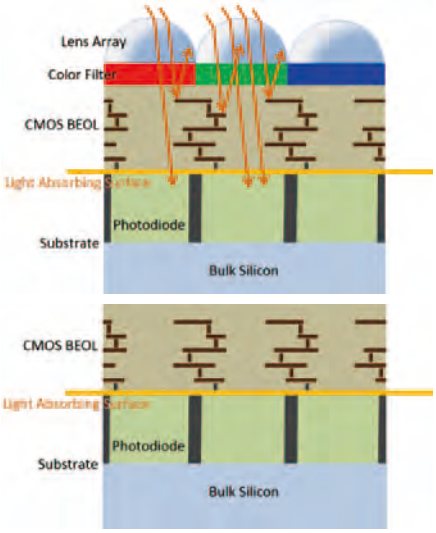


Figure 1. (Top) Front side illuminator technology vs. (Bottom) BSI using front-side processes.

The growth of the BSI market has outpaced original market expectations, and according to Yole Développment, it is expected to exceed $16B cumulatively over the next four years (**Figure 3.**)

Implication of Commerical Licensing within the Image Sensor Market

One proprietary direct bonding technology has been in existence for several years, and the technology is now gaining momentum in the market. BSI image sensors are the first real mainstream semiconductor application in the consumer electronic market space to move into the third dimension in volume production.

The fact that direct bonding technology has been licensed commercially and is in high volume production serves as confirmation of the strength of the patents covering the technology. IP companies have no choice but to protect their own intellectual property in order to survive, but when large, well-respected companies take a license, people tend to pay attention.

Other types of bonding technologies do not offer the same benefits in the area of 3D integration. The closest competition includes bonding technologies such as adhesive bonding or thermo-compression bonding. Because there is not a thick later of additional material required, direct bonding technology results in lower distortion than other technologies – a key metric for image sensor manufacturers.

The Technology

Direct bonding technology stems from more than 20 years of material research resulting in an elegant, but simple and highly efficient solution for volume manufacturing involving two or more separate substrates or devices. These processes are designed to use standard semiconductor wafer fab equipment and do not require expensive custom or specialty wafer processing equipment. Wafer bonding equipment options required for direct bonding are varied and range from relatively simple and inexpensive to much more complex. Some of the factors to consider include alignment accuracy requirements

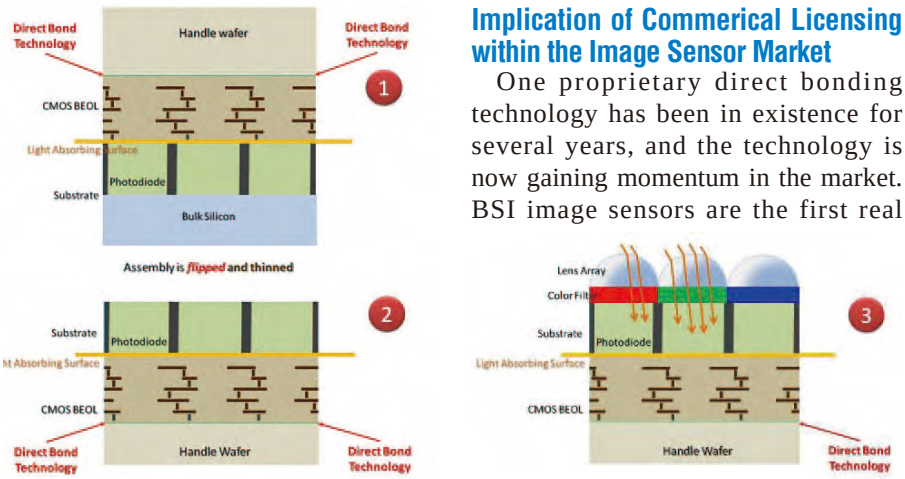


Figure 2. a) Direct bond technology b) Assembly is flipped and thinned c) Final BSI

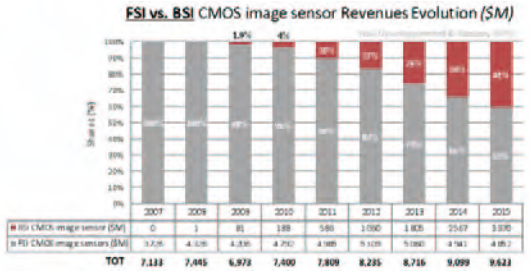


Figure 3. BSI image sensor projections presented at the Image Sensors Europe Conference in March of 2011

and level of automation required.

As mentioned, direct bonding technology is enjoying wide adoption. The patents involved are broad and involve low-temperature bonding of insulators, silicon, III-V and other dissimilar materials. The technology involves planar, homogeneous bonding surfaces, and is currently being used in high-volume manufacturing applications. Bonding can occur at relatively low temperatures due in part to a surface activation/termination step that is one component of the technology.

A second area of significant activity is direct bond interconnect and is based on the same principles as the direct bond technology, but includes conductive interconnects, so therefore involves planar, heterogeneous bonding surfaces. This technology gives customers a high-density, scalable interconnect method that leverages high-volume foundry processes. **Figure 4** is an SEM image showing the bond interface of a connection made between a pixel wafer and a logic wafer at a pitch less than 2µm. Direct bond interconnect has not yet been licensed in the consumer electronics space, so there still are opportunities for exclusivity within these markets.

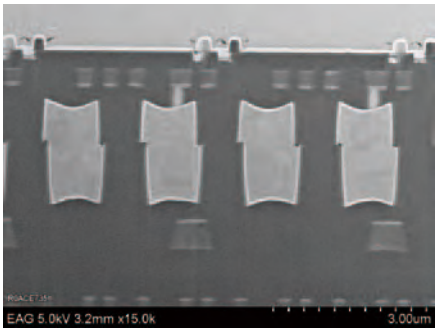


Figure 4. SEM of logic and pixel wafers' bond interface using the direct bond interconnect process

Beyond the image sensor space, there are several applications for direct bonding technology both with and without interconnects. Other applications include pico projectors, various types of stacked devices, RF front-end applications, MEMS and other heterogeneous applications.

Summary

BSI image sensors have paved the way for many 3D integration applications, some of which are already being geared up for volume production. Direct bonding is a key enabler within the 3D technology arena and is garnering much attention, both with and without interconnect, in new, advanced image sensors and a variety of other applications. Wafer stacking made possible by direct bonding is allowing chips to move out of the x-y plane and into the z-direction.

Kathy Cook, Director of Business Development, Ziptronix, may be contacted at k.cook@ziptronix.com.

IWLPC 2011 – Exploiting the 3rd Dimension

By Ron Molnar [AZ TECH DIRECT]

Jointly hosted by SMTA and Chip Scale Review, the International Wafer Level Packaging Conference (IWLPC) held October 3 – 6, 2011 in Santa Clara, CA validated the growing demand for more IC functionality in smaller IC packages by exploiting the 3rd dimension.

Figure 1. SMTA reported a 20% increase in attendance at IWLPC 2011

"The SMTA was very pleased to see a 20% increase in attendance at IWLPC." Noted SMTA Administrator, JoAnn Stromberg, "In conjunction with Chip Scale Review we were able to organize another strong technical program focused on leading-edge topics such as 3D, wafer level, and MEMS. With a sold out exhibit floor, outstanding speakers, and enthusiastic attendees we look forward to 2012 and another strong IWLPC."

This year's event, organized by Conference Chair, Andy Strandjord of PacTech USA, and Technical Chair, Luu Nguyen of Texas Instruments, consisted of 29 technical presentations organized in three parallel tracks, two panel discussions, six half-day tutorials, a poster session, two morning plenary sessions, and it was highlighted by an entertaining dinner keynote speech from Raj Master of Microsoft.

Exhibit Hall "Sold Out"

The exhibit hall was sold out this year with booths from 44 companies (up from 38 exhibitors in 2010) – prompting the hosts to move the event to a larger venue in 2012. There were 20 new exhibitors this year.

Steady supporters that have exhibited the last three years in a row include: Aehr Test, Boschman, EV Group, Kyzen, NEXX Systems, Owens Design, Pac Tech USA, Promex, Quik-Pak/Gel-Pak, Silex Microsystems, TechSearch International and Tessera.

Figure 2. John Crane of Boschman has a captive audience from Agilent

Generous Sponsors

Helping to make IWLPC the best industry conference on wafer level packaging were seven generous corporate sponsors. They were led by the Platinum-level sponsors, Amkor Technology, EV Group, and NEXX Systems. Gold level sponsors included Nanium, PacTech, STATS ChipPAC, and SUSS MicroTec.

Figure 3. At the STATS ChipPAC exhibit, Steve Wofford, Sr. director of worldwide marketing communications explains the company's latest WLP offering to an interested attendee

Amkor Technology, Inc. is one of the world's largest providers of advanced semiconductor assembly and test services. They offer a suite of services, including electroplated wafer bumping, probe, assembly and final test. Amkor is a leader in advanced copper pillar bump and packaging technologies which enables next generation flip chip interconnect.

Figure 4. Curtis Zwenger, Amkor, discusses the company's latest TSV and copper pillar flip chip technologies

EV Group, Inc. provides leading-edge wafer processing equipment for MEMS and Microfluidics, advanced packaging, compound semiconductor/MOEMS, SOI, power devices and nano-technology applications. EVGs product portfolio features double sided mask/bond aligners, wafer bonders for anodic silicon fusion, thermocompression and low temp plasma bonding, wafer/mask cleaning systems, photoresist spin/spray coaters and developers, hot embossing and nano-imprinting systems, and defect and particle inspection systems.

Figure 5. Garret Oakes, director of technology, EV Group, talks about the company's recent expansion at its world headquarters in Schaerding, Austria

NEXX Systems has pioneered economical and flexible solutions addressed specifically to wafer level packaging (WLP). NEXX has become

a global leader in the design and manufacture of advanced packaging processing systems that enable smaller and faster consumer electronics.

Figure 6. At Nexx Systems - John Bowers VP worldwide sales meets with Michael Schneider of ECI

Attendance Grows Nearly 25%

Interest and activity in the area of wafer level packaging (WLP) continues to grow. This year's conference drew 460 attendees – up nearly 25% over the 370 registrants for the 2010 event. Participation from the international community also continues to grow. IWLPC 2011 drew attendees from 15 countries – led by the United States, Germany, Japan, Korea, China and the United Kingdom.

Popular Tutorials

The organizers were proud to offer six half-day tutorials to 92 students by a number of well-known and respected industry leaders as a means of educating those unfamiliar with wafer level and advanced packaging technologies.

The two most popular tutorials were "Wafer Level Packaging" by Luu Nguyen, Ph.D. of National Semiconductor and "TSV and Key Enabling Technologies for 3D IC/Si Integration and WLP" by John Lau, Ph.D. of Industrial Technology Research Institute (ITRI).

Figure 7. Keith Cooper, SET North America, delivers an interesting talk on updated processes collective hybrid bonding for C2W processes

Talking Technical

Three parallel tracks of technical presentations were offered again this year covering WLP, 3D and MEMS topics. In total, there were 29 presentations. Judging by attendance figures, the most popular session was definitely Session 1 – Advanced Wafer Level Packaging Technologies, followed closely by

(continued on Page 42)

Innovation Trends Driving WLP and 3D Packaging

By Steve Anderson [STATS ChipPAC]

The market for portable and mobile data access devices connected to a virtual cloud access point is exploding and driving both increased functional convergence as well as increased packaging complexity and sophistication. This is driving an unprecedented demand to increase the variety of wafer level, thin POP, and TSV/interposer packaging solutions. If flip chip is the current workhorse, then we can expect to see more exciting interconnect technologies such as TSV, 2.5D interposers, FO WLP and 2nd generation FO WLP to meet these needs.

3D and Advanced Packaging Evolution

Connectivity is the key to both business and consumer electronics growth as huge investments in wireless and 3G/4G networks accelerate development of new packaging technology. Particularly important in this next generation of wafer level packaging (WLP) is the need for higher bandwidth, improved thermal dissipation and materials, and the capability for higher current per bump without creating electro migration (EM) failures.

Mobile Computing Convergence

Driven by the need for higher levels of integration, improved electrical performance, or reduction of timing delays, the need for shorter vertical interconnects is forcing a shift from 2D to 2.5D and 3D package designs. 3D integration is proceeding on three fronts, moving from the package level (die and package stacking) to wafer level, especially fan-out wafer level packaging (FO WLP), and more recently at the silicon (Si) level for through silicon va (TSV) and interposers.

Co-design between the silicon and the packaging is required to achieve an optimized cost and system solution. When co-design can be done with integrated passives, a new level of WLP can be provided that reduces costs, package thickness, and integrates more functions in a single package.

3D vs. Heterogeneous Approaches

While the need to combine more mobile functions in an efficient, low-profile solution is fueling the shift towards 3D packaging, challenges still remain in the areas of design, testing, mass production, cost effectiveness, and materials compatibility. Given that system-in-package (SiP), package-on-package (POP), and 2.5D interposer technologies have become more mature and widespread, the further deployment of embedded wafer level technologies and TSV will continue to drive the migration from 40nm to 28nm. The heterogeneous integration capabilities of these technologies is enabling a more holistic design approach by combining multiple die with memory, integrated passives, and mixed technology nodes to provide lower cost, thin profiles and more reliable, packaging solutions.

Driving forces behind wafer-level and silicon-based technologies include smaller footprint, increased functional integration, increased I/O density, improved electrical and thermal performance, and lower cost due to batch processing (**Figure 1**). Examples include:

- Fan-in wafer level bumping with tighter pitches for shorter signal lengths
- Embedded fan-out wafer level solutions
- High-speed memory and processor applications with high bandwidth interconnect that move beyond today's POP technology solutions
- Full implementation of TSV 3D packaging technology for mobile products

3D TSV technology is slated to appear in late 2013 or 2014. TSVs help enable the increased density by packing a great deal of functionality into small form factors with multiple heterogeneous functions such as logic, analog, RF, memory and MEMs. This technology provides an alternative to expensive system-on-chip (SOC) development and allows technology from different nodes to be combined in a single package.

Figure 1. Driving Forces Increasing Wafer Level Packaging Growth

Fan-Out Wafer Level Growth

Much of the initial industry work to develop and deploy fan-out WLP, (FOWLP) led by embedded wafer level ball grid array (eWLB), has been on 200mm wafers (**Figure 2**). The focus is now on 300mm formats that enable this technology to be more cost competitive and scale more efficiently. FOWLP panel sizes larger than 300mm improve the cost structure, increase production efficiencies as well as enable

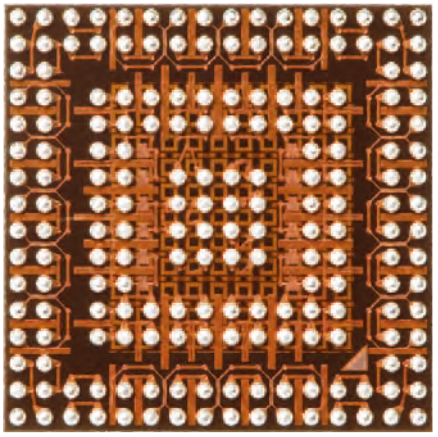


Figure 2. eWLB Fan-Out package

Next Generation eWLBs	Specification
Multi-layer RDL eWLB	More than one metal layer can be present in both sides
Thin eWLB	Package thickness is reduced to 0.5mm
Multi-chip eWLB	More than one chip is embedded
Large size eWLB	Package size is increased to 12x12mm²
Double sided eWLB with vertical interconnection	Both sides of reconstituted wafer have isolation and metal layers, connected by means of conductive vias in the plastic portion of the wafer
Small size eWLB	1x1mm small die packaging with ~3x3mm eWLB

Table 1. Key focus of next-generation FOWLP packaging development efforts

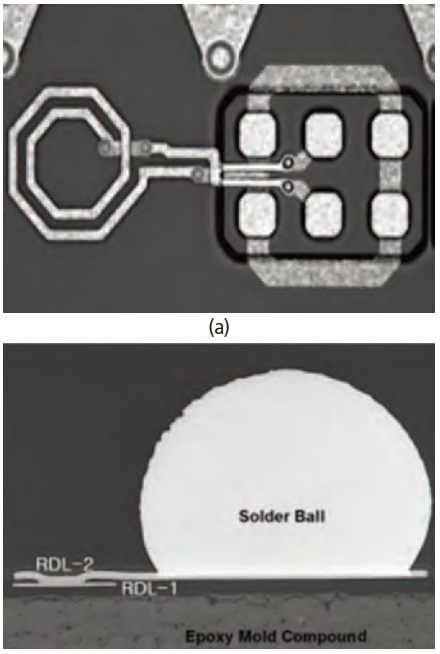
a wider range of single die and multi-die configurations. The proliferation of FOWLP configurations is expanding as the demand for increased packaging density grows, especially in 3D applications.

2nd Generation FOWLP

While first-generation FOWLP enabled very dense single and multilayer packages, new performance requirements are pushing these packaging limits toward second generation FOWLP. Achieving mainstream status for FOWLP technology status requires a broad approach with flexible, cost-effective solutions ranging from single die to multi-chip solutions in one-layer routing, to more complex multiple layers, IPD integration, POP versions and ultimately, SiP, SoP, and complete 3D solutions utilizing TSV. **Table 1** highlights some next generation eWLB packages and specifications. All of these configurations are well within the uniquely robust capabilities of this technology as a solid integration platform. The ability to route finer lines and spaces enables a wider range of packages ideal for the growing smartphone and tablet markets.

eWLB with Integrated Passives

eWLB is available in both large and small body sizes, allowing for a wide range of integration capabilities enabled by multiple layers of routing as well as vertical stacking and passive integration. (**Figure 3**). Essentially, this enables very thin side-by-side device and passive integration for powerful cost-effective systems. When vertically stacked, eWLB enables very high bandwidth and reliable high density 2.5D package solutions.



(a)

(b)

Figure 3a. Embedded inductor and **(b)** SEM micrograph of cross-section of 2-layer RDL eWLB

Multiple die FOWLP (horizontal)

The integration of one to four die along with passive functions provides significant performance, size reduction,

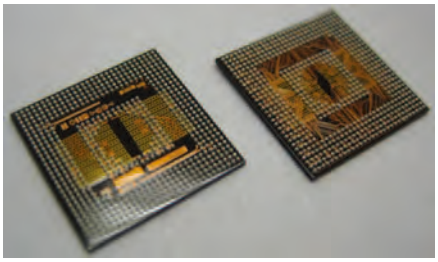


Figure 4. 12x12mm eWLB packages with two die and double layer RDL with 0.4mm pitch

and device integration critical to 2.5 to 3D system requirements of high yields and affordable price points (**Figure 4**).

As cloud computing gains prominence, new designs are emerging that require much larger FOWLP body sizes than in production today. This large die FOWLP will again push material and manufacturing requirements to have efficient panel sizes and good manufacturing process control.

eWLB POP driving 2.5D system

Low-power mobile device applications are driven by the need for increased bandwidth and speed. Putting this level of computing performance and networking capability into consumer and lower cost business systems that were once considered high-end is driving a more aggressive push towards advanced WLP solutions and 3D packaging, given the limited form factors and space required for increased battery life (**Figure 5**).

Super Thin FOWLP POP

Further integration and form factor reduction can be achieved by using a vertical FOWLP package where the die and redistribution layer serve as the interposer, eliminating costly laminate build-up substrates and providing cycle

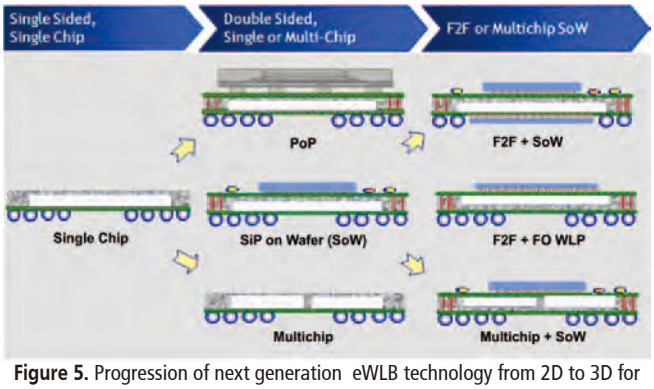
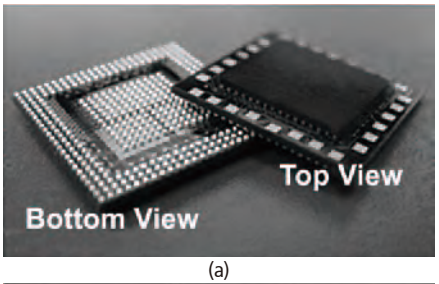
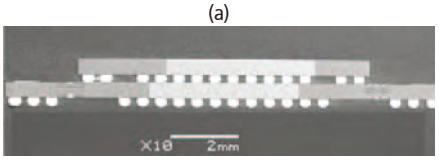


Figure 5. Progression of next generation eWLB technology from 2D to 3D for highly integrated packaging solutions



(a)



(b)

Figure 6a. Super thin FOWLP POP – adoption of FOWLP technology for 2.5D applications

time reduction. This redistribution structure reduces the stack height whereby a 12x12mm package can have a total stacked die height of less than 1.0mm (**Figure 6**). The reduced interconnect lengths will also provide better electrical performance and lower parasitic values.

Beyond Wafer Level Packaging

Increased interconnect density is driving smaller bond pad pitches, stacked die, mixed interconnect, and advanced interconnect technologies such as interposers and TSVs. Footprints are shrinking driven by reducing lithography nodes while maintaining or increasing the I/O count and driving the external ball pitch below 0.4mm down to 0.35 or 0.30mm. This trend is driving customer ball patterns to manage the escape routing and costs for system boards. Overall package performance is heavily influenced by electrical and thermal performance. The modeling and management of these functions is much more critical as more functionality is absorbed in fewer packages within these heterogeneous 3D packaging structures. System performance can be increased and improved if proper 3D packaging elements can be implemented.

FO WLP Package as TSV Interposer

Wafer level technologies such as eWLB are leading the way to the next level of thin packaging capability. They provide a robust packaging platform supporting very dense interconnection and routing of multiple die in very reliable, low-warpage 2.5D and 3D solutions. The use of these embedded FO WLP packages in a side-by-side configuration to replace a stacked package configuration, or to utilize as the base for a 3D TSV configuration, is critical to enable a more cost effective mobile market capability. A cross-section of this type of package is shown in **Figure 6**. Combining wide I/O interfaces with the TSV packaging capability can provide an optimum solution for achieving the best performance in thin multiple-die stacks aimed at high-volume manufacturing.

High-Density Solutions in a Heterogeneous Configuration

The business and consumer drive for greater portability and data on demand is forcing increased packaging density and more cost-effective 3D solutions. While POP technologies are effective for integrating functions in a small package, they lack the high bandwidth and low-profile increasingly needed by the new generation of thin tablets and more powerful mobile processors.

Technical and manufacturing issues are key challenges for 3D stacks. These include testability and yield, scalability, thermal and standardized IC interface challenges. 3D TSV packages are being developed to provide heterogeneous integration of memory, logic, graphics, and power functions that cannot be integrated into single die; and to provide improved electrical performance below 28nm from very short and high density interconnects between the stacked ICs. **Figure 7** shows an example of the transition from 2D to 2.5D and finally to 3D.

TSV Technology

TSV technology is driven particularly by the need in smartphones and tablets for much faster processing speeds and memory bandwidth in order to manage all of the advanced functions required of these products. For successful market penetration, the TSV ecosystem comprising IDM, OEM, OSAT, foundries, design houses, and PCB

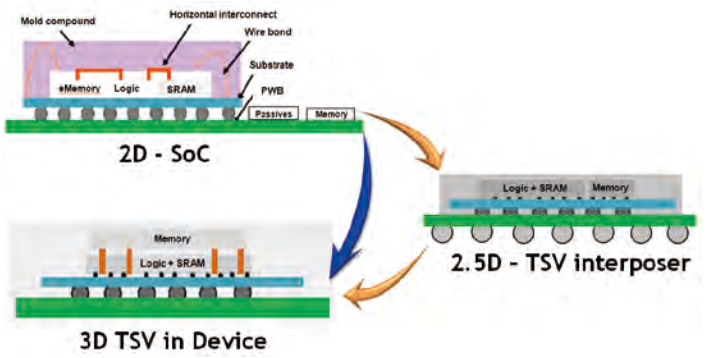


Figure 7. Transition from 2D packaging to thin 3D TSV

suppliers must be properly enabled.

The advantages of the TSV packaging approach over SOC are many including higher bandwidth due to the shorter interconnects, power reduction, lower cost, greater miniaturization and greater modularity and flexibility.

TSV Challenges and Design Requirements

Extensive retooling for design is not required to create TSV packaging. There appears to be no major roadblocks in process technology. However, new capabilities are required to route and connect fine pitch microbumps .

Package co-design and integrated process control is key for successful implementation of widespread TSV usage. While thin wafer backgrinding is available, backside TSV reveal, stealth dicing, and fine pitch thermal compression bump bonding are still under development and testing.

Conclusion

Building the 3D packaging infrastructure requires a good system to manage the IC, packaging, and the board design while trying to establish common standards for at least the memory interfaces. An ecosystem consisting of IP suppliers, foundries, OSATS, IDMS, OEMS, and design houses is being developed with co-design and standards collaboration. Cost effectiveness depends on the proper co-design of the chip, package, and board.

As the demand for mobile and portable electronics grows, the demand for smaller, lighter, and higher bandwidth packaging will grow evolving from today's POP configurations to more complex embedded WLP and vertical 3D TSV technology. Differentiation and even product success is being driven by the ever-expanding feature sets, functionality, convergence and adoption of more computing rich gesturing and graphic applications. The additional increase in cloud computing access points requiring improved packaging for the mobile networking market will only further 2.5D and 3D packaging variation adoption.

Next-generation packaging such as TSV and next-generation FOWLP is enabling these advances and proves to provide more exciting developments in the future.

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Direct Copper Bonding Of High-Density 3D Assemblies

By Gilbert Lecarpentier [SET], Marc Legros and Mayerling Martinez [CEMES-CNRS], Alexis Farcy and Brigitte Descouts [STMicroelectronics], Emmanuel Augendre and Thomas Signamarcheix [CEA-LETI], and Vincent Lelièvre and Aziz Ouerd [ALES]

Much of today's activity to develop cost-effective multilayer 3D assemblies in volume production focuses on the near-term problems and tradeoffs of vertically interconnecting stacked layers of devices and sub-systems either with through-silicon-vias (TSV) or silicon interposers. However, in 2009 the French Government took a longer-term view by funding PROCEED, a 2-year research project to increase the density of vertical connections through the use of direct copper-to-copper bonding.

The goal of the PROCEED project is to demonstrate higher density interconnects with a placement accuracy of less than 1µm for chip-to-wafer (C2W) interconnections linked by direct metallic copper-to-copper bonding. Higher connection densities will be an advantage in assembling high-performance circuits with 3D interconnections. Higher connection densities will enable a wide range of applications in microelectronics as well as in optoelectronics and in MEMS.

Direct copper-to-copper bonding requires good planarity and excellent surface quality. The controlled bonding environment has to maintain a low level of contamination from metallic particles and other sources. Both the smooth finish of the copper pillars and pads as well as the topography between the copper and oxide areas are critical to achieving good bond strength.

Direct Bonding Advantages

The C2W direct bonding process has several advantages over conventional eutectic solder bonding and thermo-compression bonding processes often considered today for 3D integration.

A major advantage of the direct bonding processes advanced by this program is very high density of the vertical interconnects it supports. Contact density may reach tens of thousands of connections per square millimeter. This is made possible both by the higher placement accuracy in direct bonding, and by the monometallic connections eliminating the potential thermal expansion mismatch stress that may occur between different metals.

Better electrical performance is attained, with lower ohmic values per unit area than older bonding approaches. The direct bonding approach provides high mechanical and electrical integrity. Unlike eutectic solder assembly, the bonding interface is void-free, resulting in lower electrical resistance, higher strength, and better reliability. The process provides robust self-sealing for C2W stacking without requiring any adhesive or underfill. C2W stacking results in higher yields than wafer-to-wafer (W2W) stacking.

The low-complexity process described here allows room temperature assembly with ambient air at atmospheric pressure. Bonding requires only low forces. That combination is an advantage in reducing line throughput time, which is essential for high-volume production.

Team Members and Tasks

The suite of skills essential for this task required the collaborative efforts of five groups, each with expert skills in some aspect of the problem: handling and bonding equipment (SET), bonding surface preparation (ALES), bonding (CEA-Leti), developing semiconductor solutions across the spectrum of electronics applications (STMicroelectronics), and assessing and comparing the results through an industrial test vehicle (CEMES-CNRS). Each partner's contributions are described here in further detail.

Equipment Development

SET created a new design configuration of pick-and-place equipment by modifying the proven FC300 platform to operate in a Class 10 environment and to meet the precision placement requirements of direct copper-to-copper bonding. This high-placement-accuracy platform has been developed as the base of the new system, designed for the special needs of the PROCEED project.

The design changes for accuracy have mainly focused on the optics and bond head stages, which move over the wafer during its population. To meet the direct metallic bonding cleanliness requirements, the system was modified to provide a low particulate contamination design that meets Class 10 environmental standards. The primary areas needing modification to achieve the required level of cleanliness were the cable channels, the mechanical housing, and the air circulation through the machine.

The main features of the modified pick-and-place equipment are its suitability to direct bonding and its alignment capability (**Figure 1**). These were assessed independently through particulate contamination measurements, transmission electron microscopy (TEM) imaging of the bonding interface, and post-bonding alignment evaluation by infrared (IR) and acoustic microscopy (SAM).

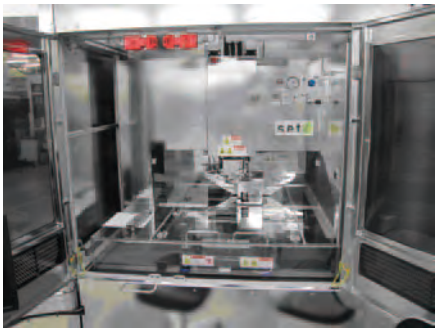

Figure 1. An inside view of the SET FC300 Bonder with direct metallic bonding configuration

Surface Preparation

Air Liquide Electronic Systems (ALES) is supplying technology to provide the required surface preparation. The approach is based on a wide knowledge of chemical-mechanical polishing (CMP) and cleaning solutions design. In this program, new chemistries were developed to meet very stringent requirements of the direct bonding surfaces (**Figures 2a** and **2b**).

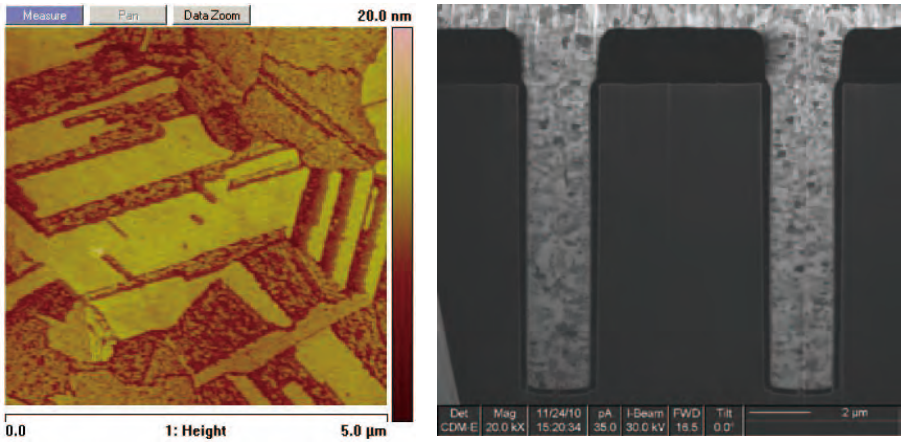

Figure 2a. AFM image of a copper surface after a one minute post CMP cleaning with chemical solutions. **(b)** SEM image of a 2 X 5 µm through-silicon via (TSV) filled with ECD copper using electroplating chemistry

In addition, development within the PROCEED project included a specific and easily adjustable dilution and distribution unit that is capable of both applying and controlling the surface preparation chemistries (**Figure 3**). Depending on the final integration scheme, this unit could be installed in the equipment in accordance with clean room specifications and mechanical requirements of the alignment process.

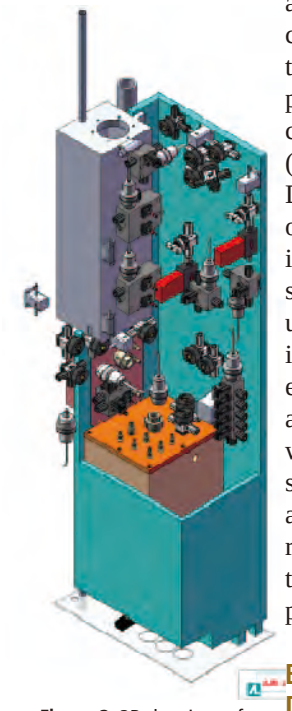

Figure 3. 3D drawings of an example of on-board surface treatment equipment

Bonding Development

In this project, CEA/LETI is fulfilling its usual role of being an interface between industry and academic research and between equipment suppliers and an integrated device manufacturer (IDM). The PROCEED project extends this activity to include 3D integrated system technologies using D2W direct bonding

A driving force for 3D integration is the need for an economically viable approach to achieve innovative multifunctional systems through the assembly of heterogeneous existing sub-parts. Through such repartitioning, sub-parts can be kept small in size, requiring few mask levels and yielding shorter interconnects, thereby improving yield, cost, performance and energy efficiency. Although 3D integration can be achieved through W2W stacking, performing C2W assembly conveys further benefits in terms of flexibility (namely in sub-part size, technology or supplier) and yield (relying on known good die (KGD) and avoiding long-range overlay issues).

Direct bonding has emerged as a powerful technique in the field of substrate engineering. When the two mirror-polished surfaces are put in contact, they are initially held together at room temperature by adhesion forces (Van der Waals forces or hydrogen bonds), without any additional materials. At that point, their adhesion is weak and the bonding is reversible. To strengthen and complete the bonding, the bonded pair is usually given a thermal treatment right after direct bonding, which causes covalent bond formation, thereby closing the interface.

Direct bonding is even more attractive for semiconductor C2W assembly. Bonding at room temperature with ambient air at atmospheric pressure avoids the time and complexity of vacuum chambers. Eliminating adhesive materials avoids handling, dispensing, and controlling liquids. Consequently, direct bonding is already in use at an industrial scale for the mass production of silicon-on-insulator (SOI) substrates. Direct bonding was also recently demonstrated with conventional damascene surfaces. These are mixed planarized surfaces that include low-pitch copper interconnects in an oxide matrix, creating conductive paths across the bonding interface. Applying damascene direct bonding to 3D integration in a C2W scheme brings in several key benefits compared to current approaches.

Copper-to-copper direct bonding enhances bonding accuracy for high-density interconnections by avoiding the potential thermal expansion mismatch of bonding different materials. To ensure void-free bonding, the alignment and bonding steps must be carried out in a particle-free environment. This is accomplished by using special materials and by careful management of the bonding environment to protect the wafer surface while it is being fully populated with dice. Because the bonding process takes place at low force and room temperature, line throughput is increased, adding capacity and reducing costs. Low-force bonding process is key to the high throughput required for widespread adoption of 3D IC integration.

The trend towards 3D integration originated in the need for an economically viable scheme to achieve innovative multifunction systems through the assembly of heterogeneous existing sub-parts. Through repartitioning, sub-parts can be kept small in size, requiring few mask levels and yielding shorter interconnects to improve yield, cost, performance and energy efficiency.

Applications Development

STMicroelectronics is driving the application of this technology for high-density 3D integration and participating in the elaboration of the specification for future high-volume machines. This role within PROCEED exists in the 3D

test chip integration for technological demonstrations of the direct bonding process. First, wafers with multiple back-end of line (BEOL) interconnect levels were provided to validate the surface preparation treatment compatibility with CMOS technology, especially considering the topology due to the presence of multiple BEOL levels. Then, a 3D test chip, which embeds several active structures, was integrated according to a full CMOS 65nm node process flow for functional demonstration. The electrical results are expected to validate both the D2W stacking tool and the direct bonding technology.

The availability of a high accuracy pick-and-place tool that meets the requirements of a direct bonding process paves the way towards a new generation of 3D integration technology. Improved placement accuracy provides higher contact density and better electrical performance compared to traditional eutectic bonding for 3D system-on-chips. Direct bonding is a core technology that provides robust self-sealing for D2W stacking. It eliminates the need for any underfill material. As shown in **Figure 4**, it enables stacking more than two die.

Combining the technologies developed within PROCEED and the results from a prior project called VERDI, which was focused on high-density TSV integration (diameter 2-5µm) and ultra-thin Si wafers stacking (thickness 10-25µm), will allow development of a full process integration flow for the next generation of high-performance 3D system-on-chips moving forward. This will enable a wider range of applications in microelectronics as well as in optoelectronics and in MEMS, including applications requiring high-density 3D interconnects, such as photonics, multimedia and wireless.

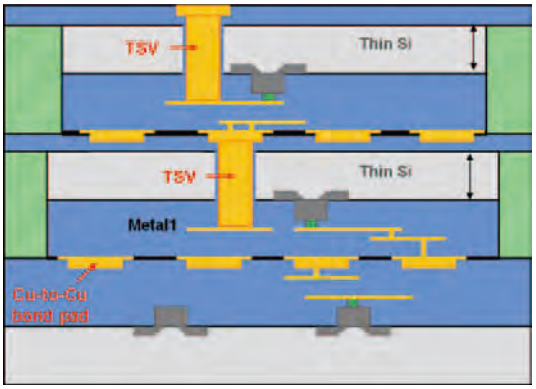

Figure 4. Three die stacking sample with copper to copper bonding pads

However, the need to first explore the challenges of providing low roughness and zero-defect surface, as well as ultra-clean D2W stacking compatible with clean room specifications, makes a research and development project like PROCEED mandatory to develop commonality in both tools and processes before ramping up this technology to industrialization.

Characterization and Metallurgy

CEMES-CNRS fills the tasks of characterizing the bonding quality and of analyzing previously unobserved changes that occur in the copper metallurgy during the annealing step. Compressive stresses or annealing steps at intermediate temperatures are known to facilitate the assembly of two wafers covered with copper films. This is a key step in creating stronger bonds for a stack of various chips in 3D. However, the mechanisms that lead to the full bonding of the copper-to-copper interface are not completely known. Investigating these mechanisms was an important part of the laboratory program.

Various forms of Transmission Electron Microscopy (TEM) were employed as the main tools in this investigation. After having annealed copper-covered wafer assemblies at temperatures of 100°, 200°, 300° and 400°C, cross-sections were cut perpendicular to the bonding interface. They were thinned down to 200µm to form TEM-observable foils.

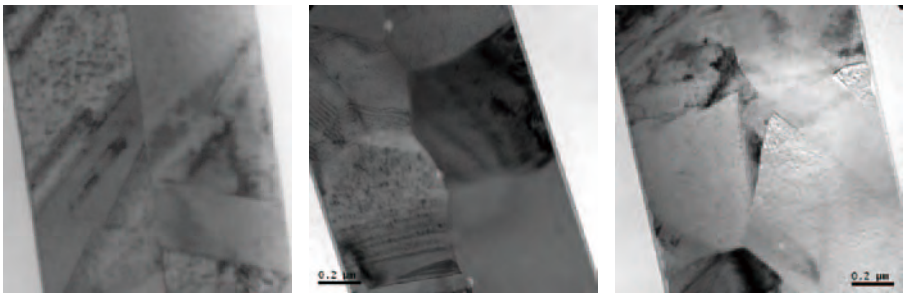

Figure 5. TEM images of the copper to copper interface after direct bonding and annealing at various temperatures. Note the decreasing flatness of the interface, especially at grain boundaries. **a)** RT to 100°C; **b)** RT to 300°C; **c)** RT to 500°C

The TEM observations clearly show that as the annealing temperature increases, the initially flat copper-to-copper interface is gradually transformed into a zig-zag shape. This change in itself leads to a stronger bond. **Figure 5** shows an example.

Directly annealing a sample inside the TEM (in situ TEM) further showed that this zig-zag shape is initiated by the rapid diffusion of copper atoms along the grain boundaries. Diffusion cones are formed at the intersection of these grain boundaries and the copper-to-copper interface, and spread until a thermodynamically stable zig-zag structure is formed.

The effect of grain orientation on diffusion is being further investigated using a new TEM Automatic Crystallographic Orientation Mapping system, purchased through the PROCEED project. **Figure 6** shows how this system is able to capture the various orientations present in the Cu-bonded interface before and after the assembly.

Results

- The pick-and-place equipment developed for this task was shown to meet the specifications and to perform well in particulate contamination control and alignment accuracy.
- Significant progress was made in the die surface preparation process, with new and more effective chemistries created. Additionally, a specific adjustable dilution and distribution system was developed for surface treatment, which could be integrated into the final equipment.

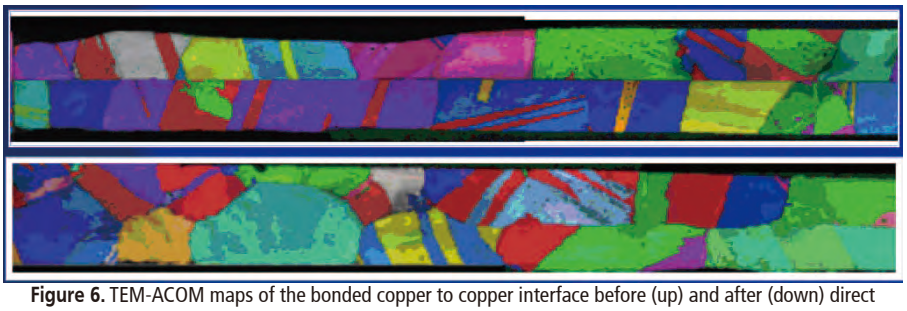

Figure 6. TEM-ACOM maps of the bonded copper to copper interface before (up) and after (down) direct bonding and annealing at 400°C. The differing colors relate to the different crystallographic orientations of the grains present on both sides of the interface

- Bonding with the new equipment and new surface treatments was successful in producing functional daisy chains with more than 10,000 contacts at a 7µm pitch, demonstrating the capability of this approach.
- A dedicated 3D test chip with embedded active structures was integrated following a full CMOS 65nm node process flow.
- Observations of metallurgical changes during annealing revealed previously unknown temperature dependent changes in surface structure by the rapid diffusion of copper atoms along the grain boundaries.

Conclusion

Project PROCEED has more than met its goals. New equipment, materials, skills and processes were combined to demonstrate that high-density copper-to-copper direct bonding is achievable and practical for 3D assembly, and has major advantages over older approaches. The demonstrations were a success and have opened the gates to further progress in high-density direct copper bonding of 3D assemblies.

Acknowledgements

The PROCEED Minalogic project is a 2.4 million Euros, 24 months undertaking supported by French FUI (Fond Interministériel Unique) with the objective of demonstrating high placement accuracy (< 1µm) of chip to wafer structures by direct metallic bonding.

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Laser Processing: A Robust Solution for Dicing Ultra-Thin Substrates

By Kip Pettigrew, Matt Knowles and Michael Smith [ESI]

The incorporation of increasingly thinner wafers is fundamental to the development of next-generation 3D packages and electronic devices. Through silicon vias (TSVs), stacked memory, 2.5D and 3D interposers, MEMS devices, system-in-package (SiP) and advanced thermal management are requiring thinner substrates to meet increased electrical needs, smaller packaging requirements, and increasingly complex designs. Silicon, the traditional base substrate for semiconductor and micro-fabrication, becomes increasingly fragile as its thickness decreases making mechanical dicing more challenging. Besides the challenge of working with thinner devices, there is a push to improve yield, develop increasingly complex stacks and better utilize wafer real estate all while maintaining cost of ownership (CoO). To address these challenges, developments for laser processing techniques for laser-only dicing are underway.

Dicing Challenges

As device wafer thickness decreases, new challenges arise when dicing. Silicon, which is normally a rigid material, becomes flexible. Below a thickness of 50µm, a silicon wafer bends like a piece of paper rather than the rigid substrate most are accustomed to. Thinner wafers have a higher probability of generating significant cracks and cleaving from the smallest of defects. Similarly, deflections in the substrate during dicing induces stress that increases the likelihood of defects and die failure.

While substrate thickness is decreasing, the associated electronics and mechanical devices are becoming increasingly complex. Dicing a semiconductor product wafer requires going through a myriad of materials that vary greatly in mechanical properties. Brittle layers such as low-*k* materials and silicon nitride are easily chipped and damaged. Thick die-attach films (DAF), which are used to package die during the assembly process, can be viscous and tacky when cut mechanically. Changes in the base substrates present an additional dicing challenge. Glass, ceramics and gallium arsenide are examples of popular substrates that are replacing silicon for many applications and present unique mechanical challenges to dice and machine.

Improving wafer utilization, eliminating process steps and minimizing costs are crucial for any electronics manufacturer to stay competitive. Any discarded part of a wafer could have accommodated an additional die and brought in revenue. Not all devices have identical footprints and it becomes progressively more challenging to singulate every die on a wafer while simultaneously minimizing waste.

Techniques for Laser Processing

Laser processing involves using a specific wavelength of coherent light to ablate material in a controlled manner. This type of processing has been widely used for many years in macro-scale drilling, cutting, and engraving. As control systems and optics have improved, laser techniques have been applied to sub-micron resolution machining such as memory repair fuse blowing, wafer & LED scribing, and wafer scoring. Taking these processes a step further, dicing techniques have been developed that cleanly cut through various electronic stacks on a wafer, the base substrate, and underlying films. Multiple wavelength types can be used to hone a specific process but for most applications described in this article a 355nm laser was used.

Traditional laser processing moves a pulsed laser beam across the substrate, ablating material as it goes. This manner of laser processing is similar to cutting a material with a saw. Slow laser processing generates heat affected zones (HAZ) that induce stress in the substrate and subsequent layers. Much like stress from mechanical processing, prolonged thermal stress can damage the electrical stack, change material properties, and jeopardize structural integrity.

To avoid these thermal effects, a "zero overlap" technique was developed to remove material along a desired dicing path. This allows heat to dissipate and thereby minimizes thermal impact and induced stress. This method precisely places individual pulses along a line at a high rate in such a way that pulses are never laid down adjacent to one another. Spacing the pulses also prevents energy losses from laser interaction with ablated

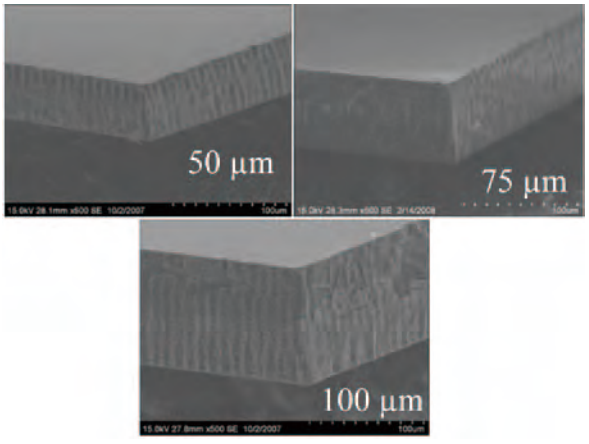

Figure 1. Laser Diced 50um, 75µm and 100µm silicon substrates

Figure 2. Laser diced device and substrate

material, and allows maximum power delivery to the target.

Precision galvo-control enables 1-2µm spot placement accuracy (relative to other spots) at up to 4.5 m/sec. Laser dicing techniques have been perfected for wafers under 100µm in thickness, while cutting through a wide variety of devices and films. **Figures 1** and **2** show cross sections of laser diced 50µm blank substrates and a scribed device wafer respectively.

Material Selectivity

Selective processing and integrating new materials into electrical devices is essential to new technology development. However, while a material may have a desired engineering property, this benefit often comes with additional processing challenges. This is commonly seen when developing processes including ceramics, glass, low-*k* materials, organic films, and rare materials such as diamond. Similarly, a device containing differing materials with drastically different properties creates the dicing challenge of not damaging any single layer while still quickly cutting through the entire stack.

Dicing in stages has been the tried and true method of dealing with material complexity, but with thinner wafers, thicker electrical stacks, and the addition of viscous materials such as DAF, a more versatile solution for all the layers simultaneously is necessary.

Laser-only dicing addresses a diverse material stack by shifting the dicing parameters (power, speed, etc.) continuously throughout the

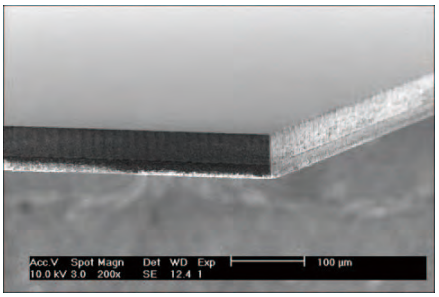

Figure 3. Example of laser dicing through very dissimilar layers: 50µm silicon and organic die-attach film

process. Parameters such as power, wavelength (355nm), speed, focus height, pulse rate and spot size (8µm 1/e2) are adjustable. As each layer of the device is diced, laser dicing parameters can be tailored to address the specific material requirements.

For example, a three stage recipe is the best approach to dice a stack consisting of standard semiconductor films and layers, a silicon substrate and a DAF. The delicate electrical components may be diced at lower power to better control the removal of thinner and fragile dielectrics and metals. After the electrical stack, the power is increased to cut through the silicon with an adjusted pulse rate to optimize throughput. Finally, when the DAF is reached, dicing parameters can be adjusted again to meet the material specifics. One could go further to use multiple lasers at different focus heights or spot sizes. The selectivity of the laser recipe's parameters to different materials could then be changed to protect some materials and target others while minimizing processing time. **Figure 3** shows a cross section of a diced wafer with device layer, silicon, and DAF.

Making the Most of Wafer Real Estate

Scribing and then cleaving silicon along the natural lattice structure is a common way to dice wafers. While cleaving works when dicing pure silicon, it becomes increasingly difficult with the addition of fragile electrical stacks and patterned features, and is limited to cross-wafer dicing and rectilinear dicing patterns. Semiconductor substrates, however, are traditionally circular. Square die result in increased waste near the wafer edge.

Laser dicing methods are not constrained to perpendicular dicing lanes. Hexagons, asymmetric device shapes, curved patterns, through holes and partial cuts are easily performed without cutting into adjacent devices or having to sacrifice wafer real estate. Examples of nontraditional dice shapes easily produced with laser dicing are shown in **Figure 4**. Hexagons are an easily repeatable pattern that better conform to the rounded wafer edges. Similarly, using a mix of octagons and squares allows for two die to be produced at the same time and have a flexible wafer footprint. Asymmetric patterns allow for a wider array of layout options as well as the flexibility to incorporate integral cooling technologies to battle the thermal challenges inherent with 3D designs.

The width of a dicing line, or kerf, has historically been set by the width of the blades needed to dice the material without excessively damaging the substrate. With laser dicing, the spot size is limited by optics and the space needed to effectively eject ablated material from the dicing lane. Dicing kerf widths of ~20-30µm cut with micron resolution precision are easily achieved when using a 355nm laser to singulate 50µm thick wafers. Thin dicing lines also free up additional real estate to the wafer. As the number of die and required dicing lanes increase, minimizing the kerf width allows for more die to fit on each wafer.

Working with Complex, SOI or Fragile Substrates

MEMS dicing is challenging because both electrical and mechanical design are critical to producing the next generation

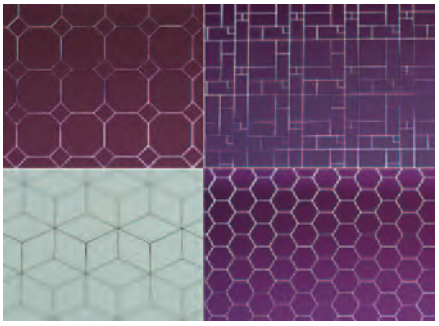

Figure 4. Laser diced die patterns with 35µm dicing lanes

of devices. Many MEMS devices such as gyroscopes and accelerometers have complex 3D structures that themselves need to be integrated into a 3D stack. Other devices, such as MEMS microphones, have fragile membranes that are easily ruptured. The laser's lack of mechanical contact enables processing on fragile substrates without any significant jarring to the wafer.

The concept of dicing should not be limited to through wafer processing. Silicon-on-insulator (SOI) wafers are commonly used to build devices on a buried oxide layer. Traditionally, the finished devices must be singulated using deep reactive ion etching (DRIE) before they are released from the buried oxide. This requires an additional masking process, involving expensive equipment on potentially delicate devices. Partial laser dicing through only the device layer of an SOI wafer is a fast and maskless process that permits the releasing of devices without additional lithography, vacuums, or post processing.

For complex MEMS devices, laser processing has the advantage of being able to cut on any plane parallel to the wafer surface. Material can be removed from the center of a recessed area by shifting the focus of the dicing beam, eliminating the need for a mask or complex 3D lithography. Holes can be diced into the middle of a die at the same time as the primary dicing lines, saving process steps and lead time. Step etching and generating through holes in a device are common processes, especially in fluidic designs and integrated cooling solutions.

Maintaining Die Break Strength

Die break strength (DBS) is commonly characterized using a three-point bending test. Chips and defects in the die result in faster fracture of the substrate and a lower DBS. Laser dicing, when running at high dicing speeds, can produce small defects in the substrate akin to mechanical dicing at high velocities. These defects lower the DBS of the die and must be addressed in post processing to eliminate this concern.

There are several ways currently used to address the DBS weakening in thin substrates either by annealing the die or by "healing" the areas where damage may have occurred. As part of the post laser dicing process, a short XeF_2 etch may be used to remove thermally stressed HAZ material and improve overall die performance. XeF_2 preferentially etches exposed silicon and stressed areas. A post-etch chamber was integrated to the laser dicing tool to minimize processing time and maintain high throughput.

Laser-diced wafers without any post processing have minimal chipping and somewhat lower DBS as compared to mechanical techniques, typically of order 250MPa. With the added XeF_2 post processing, DBS over 500MPa are easily achieved.

Weighing the Pros and Cons

There are pros and cons to using laser processing that largely depend on the devices being singulated. The biggest limitation is the thickness that one can dice quickly with a laser. As wafers get thinner, the speed at which a traditional saw dices a wafer must decrease to minimize damage to the substrate. Conversely, the thicker the wafer, the more passes it takes a laser to dice completely through the substrate. Evaluating silicon wafers, the CoO, and potential for wafers diced per hour, laser vs. saw dicing are competitive at a wafer thickness of 50µm with rectangular die, all other things being equal. The general trend of this CoO vs. wafer thickness is shown in **Figure 5**.

For wafers with a thickness greater than 50µm, specific device requirements such as non-rectangular die or mixed use applications may still drive customers to select laser processing over saws. As mentioned throughout this article, there are advantages to both and ultimately the requirements and materials of the device stack must be considered to determine the best dicing option.

Conclusion

As devices become increasingly complex and micro-fabrication becomes more competitive, it is crucial to continually develop new tools and solutions to allow innovative designs to come to fruition. Laser dicing is a robust solution to the challenges of thin-wafer dicing, working on fragile substrates, maximizing wafer real estate and permitting the inherent creativity required to meet the needs of a demanding electronics market.

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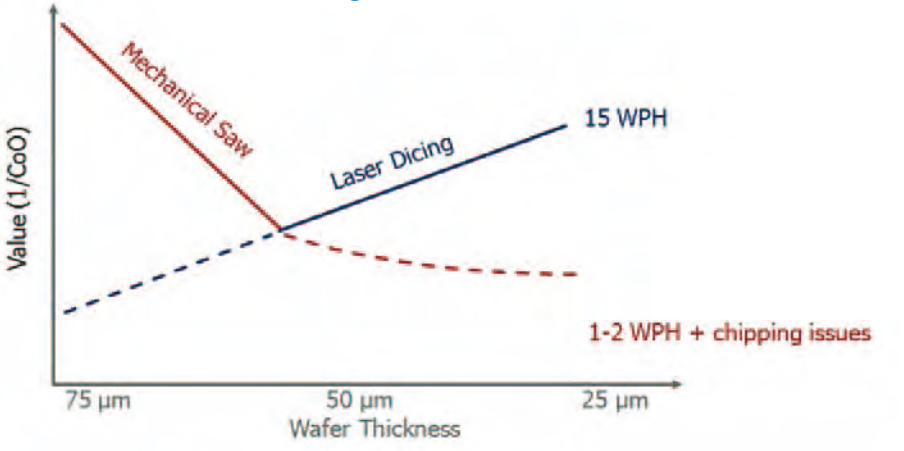

Figure 5. Laser verses mechanical dicing Cost of ownership as a function of wafer thickness

Solder in the Age of 3D Semiconductor Assembly

By Dr. Andy C. Mackie, Global Product Manager and Tae-Hyun Park, Country Sales Manager [Indium Corporation]

The cutting edge of the semiconductor packaging industry is seeing what is probably the largest series of simultaneous changes in both its assembly methodologies and basic infrastructure since the move from thermionic valves to silicon over fifty years ago. The advent of 2.5D and 3D assembly processes is accompanied by significant process complexities caused by through silicon vias (TSVs), thinned die, 450mm wafers, ever more fragile interconnect-layer dielectrics, and the criticality of doing all this while maintaining acceptable yields. The relentless driver is the "price-elastic growth of the electronics industry" [1], the basic principle behind Moore's Law [2].

One common factor underlies these changes: there must be reliable electrical interconnects between the devices. It is becoming apparent that extant materials and processes are evolving to meet the challenges; providing extensions of known quantities, rather than relying on the process engineer to implement yet one more change amongst many. As has been pointed out, "the essential process in [all] solder joining is the chemical reaction between [substrate metallization] and tin to form intermetallic compounds having a strong metallic bonding" [3].

The focus of this paper is solder and flux usage in these more advanced technologies, with special focus on those processes where solder is immediately adjacent to the die surface. As will be seen, despite competing gas-phase[4] and solder-free[5] processes, flux and solder are definitely not going away in the near term.

Flip-Chip Background

The history of flip-chip assembly goes back to the earliest days of tape automated bonding and the IBM C4 process[6]. Market projections show that flip-chip wafer starts for combined copper pillar and solder bump flip-chip for the top 14 companies is showing an 18.6% annualized growth rate[7] from 2009-2012, with growth in copper pillar as the main market driver. Table 1 shows several means of putting solder onto underbump metallization (UBM) pads.

One processor manufacturer announced that for many of their multicore die, the I/O pitch will see a modest reduction from 180µm to 165µm pitch for the foreseeable future, and will continue using standard flip-chip assembly processes. Meanwhile, their portable products are already at the 40µm pitch node using copper pillars, and will presumably shrink in pitch further into the future.

Solder Application Method	Common Usage
Solder paste printing (paste type 5,6,7,8)	Wafer and substrate (SOP) bumping down to 125µm pitch
Flux print and solder ball-drop	Wafer level CSP down to 0.3mm pitch, and some wafer bumping down to 80µm pitch
IBM / Suess C4-NP (liquid solder)	Wafer bumping down to 20µm pitch or less
Solder plating	Wafer bumping down to 20µm pitch or less

Table 1. Solder application methods

Copper pillars on wafer surfaces are almost always capped with "microbump" solder. Although there are some instances in larger pitch applications (80µm and above) where pure tin (Sn) has been used as a microbump solder, the most common solder in this application is an off-eutectic tin/silver (Sn/Ag) alloy, which is most often applied by plating since it is then just the final plated layer in a sequence. The alloy target ranges from 1.5 to 2.5% Ag, depending on the plating process control capability and the desired metallurgy of the final reflowed joint.

The standard method of turning the often misshapen solder deposits into coplanar, hemispherical microbumps [**Figure 1**], is to use a semiconductor-grade wafer bumping flux after the final resist-strip step, followed by cleaning. The flux is applied to the wafer surface like a photoresist by a spraying/dispensing process, then "spun down" to produce the desired thickness. For some wafer bumping houses, the high-aspect ratio of microbumps on copper pillars has necessitated some changes in the way wafer bumping fluxes are applied, making flux rheology a much more critical control parameter.

Resin-based fluxes are essential for high-melting alloys and have been the traditional means of reflowing 90Pb/10Sn and 95Pb/5Sn solder bumps. With these alloys, even at the very low oxygen levels used for wafer bumping flux reflow (usually less than 10ppm O_2) water-soluble flux chemistries remain difficult to clean. However, as "eutectic" (63Sn/37Pb) and tin/silver (Sn/Ag) bumps have become prevalent, water-soluble fluxes have become the standard.

Note that although there are known instances where a reactive atmosphere approach may be used to reflow solder bumps[8], the limited capability of

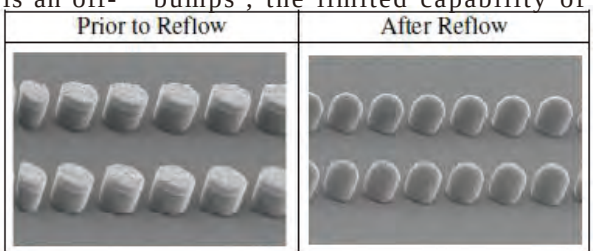

Figure 1. Wafer-Bumping flux turns the misshapen solder deposits into coplanar, hemispherical microbumps (Courtesy of Amkor)

the process to has led to significant resistance to adoption for finer-pitch wafer bumping applications. Just some of the technical issues reported are[9]:

- "Soccer ball" sphere shape defects
- Oxides and organic/residual photoresist contamination
- Inability to remove wafer probe-marks

Each of these defects can, of course, play a role in subsequent voiding during flip-chip assembly.

Flip-Chips and Interposers

So-called 2.5D (interposer-based assembly) is an enabling technology for the increasingly fragile ultra low-k (ULK) dielectric materials in the interconnect layer on the chip surface. The interposer essentially replaces the use of capillary underfills as a primary stress reliever for chips fabricated with sub-32nm devices. However, underfill will probably still continue as an added reliability enhancer in the chip-interposer stack up. The interposer is usually either itself made of silicon, or a glass/ceramic material with a CTE close to that of silicon. By matching CTEs, the interposer reduces the stress on the microbump interconnects. The processes used for forming low-oxide, coplanar solder bumps on interposers are exactly the same as those used for forming solder bumps on wafers, with plating being predominant.

Standard Flip-Chip Attach Processes

In flip-chip die-attach processes, two kinds of flux may be used (**Figure 2**):

1. A low viscosity flux sprayed or jetted onto the substrate is very effective for smaller die with high I/O counts, as long as wetting onto the substrate is consistent. These fluxes typically have low solids content and can be easily cleaned off, even with tighter pitch constraints. By using a heated spray nozzle, a higher solids-loading flux can be applied with a lower viscosity, yet on cooling is viscous enough to prevent drift and skew of larger die.
2. Dipping the solder bumps on the chip into a flat reservoir of more viscous flux of a controlled depth is more suited to larger (multicore) die. Improvements in process control of doctor-blading and dipping processes, along with specialized flux chemistries, mean that a stable dip depth down to as low as 10µm can now be consistently guaranteed for rotary systems. The subsequent reflow process is carried out in a reflow oven at less than 50ppm oxygen.

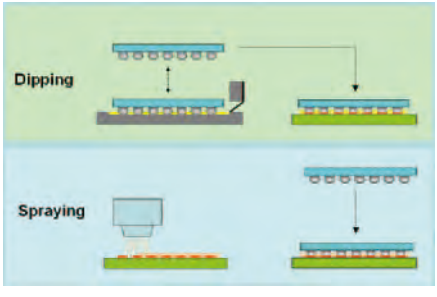

Figure 2 . In flip-chip die-attach processes, two types of flux may be used

By combining processes 1 and 2, it is possible to get a flip-chip assembly process that avoids intermittent contact non-wet (CNW) issues, has zero die skew, and is insensitive to incomplete spray flux wet-out onto varying substrate photoresist surfaces.

Although uncommon, one large processor manufacturer even uses a high-viscosity flux: printing it directly onto the substrate before flip-chip attach and reflow.

Copper-Pillar Flip-Chip and Die-Bonding

Die to die (D2D) is the preferred assembly process and is capable of high-yield manufacturing. The process uses either standard flip-chip assembly and reflow, or thermocompression bonding (TCB). The term TCB as applied to flip-chip bonding is relatively new[10], although the tooling has been available for a number of years. As an example of the extensibility of current processes, one Taiwanese OSAT has established a 40µm pitch microbump D2D process using a dipped flip-chip flux. The keys to the success of the flux are the flux rheology and the solubility of the post-reflow residue in deionized water.

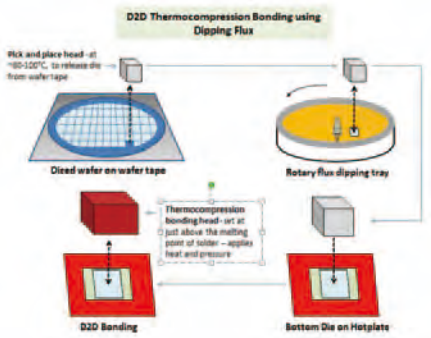

Figure 3 . One of the ways in which TC bonding is being implemented for D2D assembly

The reflow process is carried out in a controlled atmosphere using a Japanese thermocompression bonding tool, and cleaning with deionized water and an added cleaning chemistry to reduce surface tension.

The move from standard oven-based flip-chip reflow processes to TCB for 3D assembly is based on several different factors, but the primary difference is the issue of surface tension of small solder bumps. The addition of pressure to the reflow bonding process ensures elimination of "head in pillow"-like defects, or CNW.

Figure 3 shows just one of the many different ways in which TC bonding is being implemented for D2D assembly. The TC bonding head temperature setting is usually just above the melting point of the solder, so minimal brittle tin/copper intermetallics are formed, and solder joint starvation caused by solder wetting up and down the copper pillars is also minimized. The bonding pressure also has to be optimized to prevent CNW issues (too low pressure) and solder "squeeze out" (too high pressure)[4].

As I/O pitches decrease below 40µm (for D2D and D2W applications), cleaning

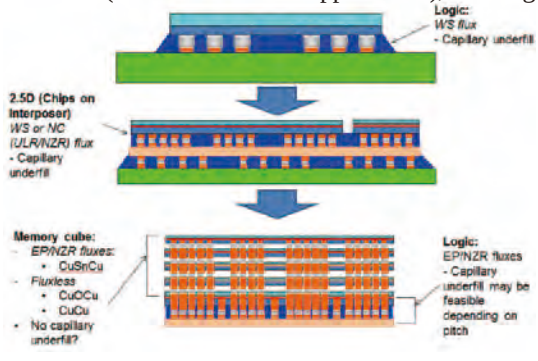

Figure 4 . Flux applied in standard flip-chip, 2.5D (interposer) and future 3D (memory cube on logic) assembly

out flux from between the stacked die becomes impractical for all but the smallest die. Capillary underfill, as well as other types of non-conductive underfilling approaches[11], will still be needed to ensure reliable electrical interconnects into the foreseeable future. Any flux residues must either encapsulate the joint and provide added joint strength (epoxy fluxes), or be compatible with subsequent underfill processes.

For standard no-clean fluxes, the presence of even ultralow (3-4%) residue (based on initial flux mass) levels may be enough to block capillary underfill flow, and so 30µm pitch and less 2.5D applications are moving to either near zero residue, <2% (NZR) no-clean dipping or spraying fluxes, or dipping epoxy fluxes.

D2W

Die to wafer (D2W) assembly for 3D heterogeneous integration may also benefit from water-soluble fluxes, although the presence of adjacent die on the surface makes both cleaning and underfilling more complex. D2W processing is a less common assembly method, a fact that may be related to subsequent difficulties related to handling and dicing of the thinned wafer.

W2W

The current understanding is that wafer-to-wafer (W2W) bonding will be used primarily to manufacture the multi-stack die for so-called "memory cubes", since the die are all the same size. The standard W2W bonding processes for TSV stacking are:[12]

- Copper / Copper (high temperature)
- Copper / Copper oxide / Copper (moderate temperature)
- Copper / Tin / Copper (much lower temperature)

The first two processes are solid-state diffusion bonding processes. The last of the three (a transient liquid phase intermetallic process) is a target for a no-clean flux-based process using a jetting, dipping, or similar deposition technology. Cleaning materials out from between the bonded wafers is clearly impossible for standard cleaning processes, although supercritical fluid approaches may be feasible.

imec has stated that by 2015, stacked wafers, such as those used in memory cube applications, will have W2W clearances of only 500nm (0.5µm). Thermal issues will be the primary concern here, and alternatives are already being planned.[13] **Figure 4** shows the way that flux may be used and applied in standard flip-chip, 2.5D (interposer) and future 3D (memory cube on logic) assembly.

3D in Power Devices

Decades ago, power electronics consisted entirely of discrete components, with the die adhesive-bonded or soldered to the main leadframe backplane, and wire bonds to the top surface. The solder

used in these instances has typically been either a clean, oxide-free (SSDA) wire that is applied by a special machine that feeds the wire onto the heated leadframe in a forming gas (H2/N2) atmosphere, or a dispensed solder paste that is also often reflowed in forming gas or nitrogen, then cleaned. Low cost, high temperature-tolerance and reliability are key factors for the interconnect material, which explains the continuing usage of solder here.

Power electronics in the 2010s also includes LED's, GaN die and IGBT modules, with different form factors, and changes such as multiple thick aluminum wire bonds (and even flexible circuitry) to the top surface. Meanwhile, the electrical interconnect requirements remain fundamentally the same, but with an increasing drive towards increased service life; higher operational temperatures (200°C is now becoming a need); and the corollary of more extreme thermal cycling.

By their very nature, since many power semiconductor devices are designed to pass current in the Z-axis through the chip, it has always been feasible to stack these devices on each other, using a thin leadframe interposer "clip". Such packages are truly 3D chip stacks, per the JEDEC definition.[14] The thinner packages eliminate wire bonds: getting rid wire-loops, and also significantly increasing the current-carrying capacity.

Power management devices in portable electronics need to be of small and low profile form factor as much as their digital cousins. Power components therefore also rely on thinned die and the use of flat clips (**Figure 5**) rather than "bulky" thermosonic ball and wedge wirebonds. The use of clips also eliminates extra process steps by combining all reflow in a single process. Solder pastes with residues compatible with overmolding compounds have been used in clip-bonding applications, so that even the residue cleaning step can be eliminated.

Lead-free (Pb-free) alloy development is of critical concern and we are nearing completion of a major project on Pb-free solder wire for automotive stacked-die power semiconductor products.

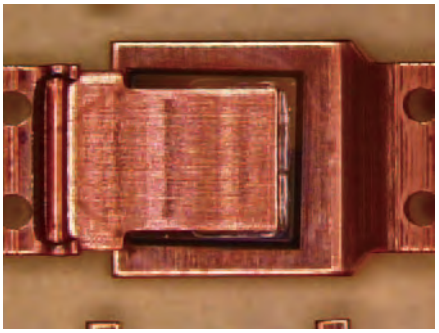

Figure 5 . Power components rely on thin die and flat clips for interconnect

Product Quality

Finally, OSATs and others engaged in semiconductor packaging are becoming increasingly aware that product quality is a key part of supplier qualification for semiconductor-grade solder paste and fluxes. There are myriad failure modes, but the primary issue is one of correlating the measured quality parameters of the material to the final functionality, especially in emerging applications such as 2.5D and 3D interconnect. Some of the more critical issues here are:

- Flux and paste rheology
- Solder powder particle size distribution
- Halogen-content[15]
- Surface insulation resistance(SIR) and electrochemical migration
- "Particles" – gel, crystals, foreign matter and so on
- Controlled (low and ultralow) alpha particle emissions

Both users and suppliers also face the formidable issue of an absence of applications-relevant test methods for many of the above properties. It is usually assumed by both sets of parties that "standard" (often assumed to be IPC[16]) standards and test methods, designed primarily for SMT assembly materials, are extensible to semiconductors. Increasingly, they are not.

In the midst of this uncertainty, it is therefore critical to be able to partner with suppliers who are leading the industry in development of testing methodologies, and who can truly supply "semiconductor grade" materials.

References

1. W. Bottoms: Presentation "Roadmaps and the Revolution in Packaging", MEPTEC Roadmap Packaging Meeting 2010, p. 22
2. http://arstechnica.com/hardware/news/2008/09/moore.ars
3. King-Ning Tu "Solder Joint Reliability" Publ. Springer, 2007, p. 1
4. Zhan et al. "Development of Fluxless Chip-on-Wafer Bonding Process for 3DIC Chip Stacking with 30micron Pitch Lead-Free Solder Micro Bumps and Reliability Characterization" ECTC 2011
5. M. Knoerr and A. Schletz, "Power SemiconductorJoining through Sintering Silver Nanoparticles" CIPS Conference 2010
6. K. Gilleo "Flip-Chips Tutorial 6" http://www.flipchips.com/tutorial06.html
7. J. Vardaman et al., "2010 Flip-Chip and WLP: Market Projections and New Developments", Techsearch International Report
8. Wei Lin and Y. C. Lee: "Study of Fluxless Soldering Using Formic Acid Vapor", IEEE Transactions on Advanced Packaging, Vol. 22, No. 4, November 1999
9. Data from three separate Taiwanese customers' experiences: further details were shared with author in confidence
10. http://blogs.indium.com/blog/semiconductor-and-power-semi-assembly/thermocompression-bonding-for-microbump-flip-chip
11. M. Kelly and W. Do, "3D Packages with TSV Silicon Interposers", TP-11, iMAPS Arizona, February 2011
12. P. Garrou, "3D IC Integration: Status and Overview" PDC, iMAPS Arizona, February 2011
13. http://www.electroiq.com/blogs/insights_from_leading_edge/2011/09/iftle-66-3m-ibm-seek-to-improve-thermal-underfills-tsmc-in-back-end-packaging-again.html
14. JEDEC Publication JEP158 "3D Chip-Stack with Through Silicon Vias…" p. 4
15. JEDEC/ECA Joint Standard: JS-709 "Defining Low-Halogen Passives and Solid State Devices (Removal of BFR/CFR/PVC)" – August 2011, but currently under revision.
16. IPC "The Association Connecting Electronics Industries": http://www.ipc.org

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International Directory of Solder and Flux Suppliers

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	FLUX PRODUCTS	SOLDER PRODUCTS	BGA/CSP SOLDER SPHERES
Company Street Address City, State, Country Telephone Website CM = Contact Manufacturer	***Chemistries*** Halide Free (HF) No Clean (NC) Rosin (R) Rosin, Activated (RA) Rosin, Mildly Activated (RMA) VOC Free (VF) Water Soluble (WS)	***Alloys*** Leaded (PB), Lead Free (LF) Low Alpha (LA) ***Forms*** Anode (A), Bar (B), Foil (F) Paste (Pa), Powder (Po) Preform (Pr), Sphere (S) Wire - Cored (CW), Solid (SW)	***Specifications*** Alloys Sphere Diameter Diameter Tolerance Melting Point
AIM 9100 Henri Bourassa Est. Montreal, Quebec H1E 2S4, Canada Tel: +1-514-494-2000 www.aimsolder.com	HF, NC RA, RMA VF, WS	PB, LF A, B, F, Pa, Po, Pr, S CW, SW	Alloys: PB, LF Diameter: CM Tolerance: CM Melting Point: 138 - 356°C
AMTECH (Mfg. by SMT International, LLC) 500 Main Street, Suite 18, P.O. Box 989 Deep River, CT 06417 Tel: +1-860-526-8300 www.amtechsolder.com	HF, NC RA, RMA VF, WS Other	PB, LF B, Pa, Po, Pr, S CW	Alloys: PB, LF Diameter: 3 - 45 mils Tolerance: CM Melting Point: CM
BALVER ZINN Josef Jost GmbH & Co. KG Blintroper Weg 11 58802 Balve, Germany Tel: +49-23-759150 www.balverzinn.com	NC RMA VF, WS	PB, LF A, B, F, Pa, Po, Pr, S CW, SW	Alloys: CM Diameter: CM Tolerance: CM Melting Point: CM
Bow Electronic Solders (Div. of Kaydon Corp.) 1 Crossman Road Sayreville, NJ 08872 Tel: +1-732-316-2100 www.solders.com	HF, NC R, RA, RMA VF, WS	PB, LF B, F, Pa, Pr, S CW	Alloys: PB, LF, Metal Core, Cu Diameter: 1 mil Min. Tolerance: +/-0.2 mils Melting Point: CM
Cookson Electronics, Semiconductor Products 3950 Johns Creek Court, Suite 300 Suwanee, GA 30024 Tel: +1-678-475-6900 www.cooksonsemi.com	HF, NC WS	PB, LF Pa, S	Alloys: PB, LF Diameter: 10 - 35 mils Tolerance: +/-0.5, 1.0 mil Melting Point: 179 - 302°C
DKL Metals Ltd. Avontoun Works, Linlithgow West Lothian, Scotland EH49 6QD Tel: +44-1506-847710 www.dklmetals.co.uk	HF, NC RA, RMA VF, WS	Pa, S B, Pa CW, SW	
EasySpheres 12675 Danielson Court, Suite 403 Poway, CA 92064 Tel: +1-858-486-4068 www.easyspheres.com	WS	PB, LF S	Alloys: PB, LF Diameter: 0.2 - 1.0 mm Tolerance: CM Melting Point: 179 - 302°C
Fukuda Metal Foil & Powder Co., Ltd. 20, Nakatomi-cho, Nishinoyama, Yamashina-ku Kyoto 607-8305, Japan Tel: +81-75-593-1590 www.fukuda-kyoto.co.jp		LF Po S	Alloys: LF, Cu Core Diameter: 80 - 760 um Tolerance: +/-10, 20 um Melting Point: 190 - 227°C
How Tsen Int'l Electronics Metal Co., Ltd. No. 12, Ln. 130, Sec. 2, Zhung San E. Rd., Sin Wu Taoyuan, 327 Taiwan Tel: +886-3-477-7517 www.howtsen.com		PB, LF S	Alloys: PB, LF Diameter: 70 - 889 um Tolerance: +/-5, 10, 15, 20 um Melting Point: 133 - 227°C

International Directory of Solder and Flux Suppliers

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	FLUX PRODUCTS	SOLDER PRODUCTS	BGA/CSP SOLDER SPHERES
Company Street Address City, State, Country Telephone Website CM = Contact Manufacturer	***Chemistries*** Halide Free (HF) No Clean (NC) Rosin (R) Rosin, Activated (RA) Rosin, Mildly Activated (RMA) VOC Free (VF) Water Soluble (WS)	***Alloys*** Leaded (PB), Lead Free (LF) Low Alpha (LA) ***Forms*** Anode (A), Bar (B), Foil (F) Paste (Pa), Powder (Po) Preform (Pr), Sphere (S) Wire - Cored (CW), Solid (SW)	***Specifications*** Alloys Sphere Diameter Diameter Tolerance Melting Point
Indium Corporation 34 Robinson Road Clinton, NY 13323 Tel: +1-315-853-4900 www.indium.com	HF, NC R, RA, RMA VF, WS	PB, LF B, F, Pa, Pr, S CW, SW	Alloys: PB, LF Diameter: 0.1 - 1.27 mm Tolerance: +/-10, 15, 20 um Melting Point: 183 - 302°C
Kester, Inc. (an Illinois Tool Works Co.) 800 West Thorndale Avenue Itasca, IL 60143 Tel: +1-630-616-4000 www.kester.com	HF, NC RA, RMA VF, WS	PB, LF B, Pa, Pr CW, SW	
Nihon Superior Co., Ltd. NS Bldg. 1-16-15 Esaka-cho, Suita City Osaka 564-0063, Japan Tel: +81-6-6380-1121 www.nihonsuperior.co.jp	HF, NC RMA WS	PB, LF A, B, Pa, Pr, S CW, SW	Alloys: PB, LF Diameter: 0.1 - 0.76 mm Tolerance: +/-5, 10, 20 um Melting Point: CM
P. Kay Metal, Inc. 2448 E. 25th Street Los Angeles, CA 90058 Tel: +1-323-585-5058 www.pkaymetal.com	HF, NC R, RA, RMA VF, WS	PB, LF B CW, SW	
Pure Technologies 177 U.S. Hwy 1, Suite 306 Tequesta, FL 33469 Tel: +1-404-964-3791 www.puretechnologies.com		PB, LF, LA A, F Po, Other	
Qualitek International, Inc. 315 Fairbank Street Addison, IL 60101 Tel: +1-630-628-8083 www.qualitek.com	HF, NC RA, RMA VF, WS	PB, LF B, Pa, Po, S CW, SW	Alloys: PB, LF Diameter: 10 - 35 mil Tolerance: +/-0.5 - 1.0 mil Melting Point: 183 - 302°C
Senju Metal Industry Co., Ltd. Senju Hashido-cho 23, Adachi-ku Tokyo 120-8555, Japan Tel: +81-3-3888-5151 www.senju-m.co.jp	HF RA, RMA WS	PB, LF B, Pa, Pr, S CW, SW	Alloys: PB, LF, Cu or Ag Core Diameter: 0.02 - 0.76 mm Tolerance: +/-3 - 20 um Melting Point: 183 - 302°C

Test Improvement via Electroless Plating

By Terence Collier [CVinc.]

Aluminum die pads will always lead to yield loss. Its inevitable. Aluminum pads form natural oxides that are accelerated by fab and assembly processes. Stick a piece of fresh aluminum in oxygen and it will quickly grow 20Å-50Å of Al(O) in some form or fashion. Add a little fluorine from a plasma asher and it will grow around 250Å to 500Å. Place it in the wafer saw and you might find up to 1000Å. If one is not careful, electrically conductive aluminum might not be detected until 150Å to 200Å understand fab processing conditions.

Depending on which probe technology is chosen, it might be difficult to achieve yields that reflect 85% of known good die (KGD). There are probe technologies that use cantilevers and others with straight/blunted needles. Cantilever probes scrape across the pad, removing the top contamination layer of the pad to make electrical contact with the subsurface electrically conductive aluminum

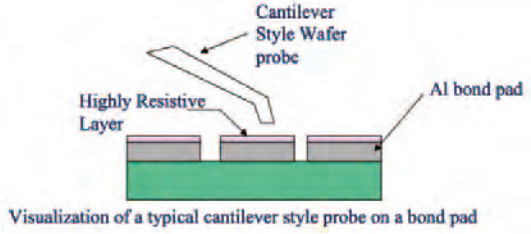

Figure 1. Example of a cantilever probe

(**Figure 1**). This displacement technology can damage pads and the under lying structures. There is also a limit on the pad size and spacing with cantilever technology.

Vertical probes minimize the scraping motion and allow for smaller pad size and pitch. Whereas cantilever probing occurs primarily in the X-Y direction with some Z travel, most of the travel with vertical probing is in the Z-direction. Unfortunately, vertical technology relies on probe displacement of pad material in the X and Y direction. Just like stepping in mud, smearing does not displace all the material in the path of penetration. Therefore, a combination of cantilever and vertical probing is a good solution, but probes are costly, and there is still some yield loss at probe and more yield loss at assembly due to additional saw corrosion. So how does one completely eliminate the issue of bond pad corrosion and mitigate the yield loss minimized optimum electrical test?

It is important to first identify the root cause, then review the process constraints and propose a solution. The solution should not add more cost to the wafer than the yield loss, or additional cycle time gained with reprobe of wafers (reprobe will be explained later). The solution should be easy to implement and not impact the fit, form, or function of the product. Most fabs do not wish to make any changes that will lead to requalification (internally or by the customer). Requalification of product is both timely and expensive. Even changing probe technology can lead to requalification since pad parameters can change (probe marks "damage" the pad and change the way wirebonds stick to the pads).

Root Cause

As stated earlier, corrosion on the pads begins in fab processing (**Figure 2**). One of the last stages is die passivation with protective oxide (nitride, oxide or oxynitride). That oxide is opened with fluorine plasma, which imbeds itself into the aluminum metal matrix. The fluorine serves as a catalyst to promote accelerated bond pad corrosion. Instead of a typical 50Å corrosion layer of oxides, the thickness can grow to a spongy layer up to 500Å. At this point, probing proves difficult. Removal of

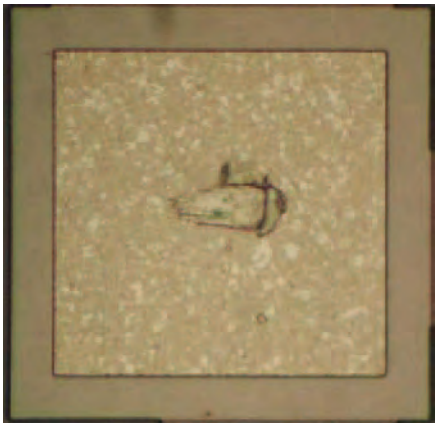

Figure 2. Optical image verifies that Al (white) is sparse and that there is Fluorine corrosion regrowth in the probe mark

the corrosion that affixes to the probe needles leads to increased probe yield loss as this material is difficult to remove from the probe needles as well as the bond pads.

Process Constraints

What are the constraints? The fab is not going to change the fluorine etch gas. Improving yield requires removal of the corrosion layer without interfering with probing or requiring new qualifications in fabrication or assembly. So the process constraints are that the fluorine etch gas will not be changed and the probe technologies will not be modified (or cannot be modified). As long as fluorine is present, the corrosion layer will continue to grow (**Figure 3**).

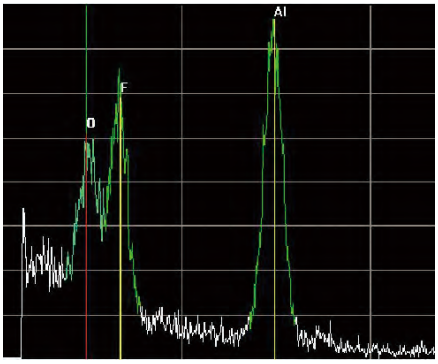

Figure 3. Notice the area under the curve shows more OF corrosion (oxyfluoride) than pure aluminum

Contact resistance (CRES) is directly related to the degree of bond pad oxidation, contamination, and corrosion. Reducing CRES improves both assembly and test yield. With high CRES, false failures occur during testing as probe needles come in contact with non-conductive CRES layers. Penetrating this CRES layer requires higher force on the probe needles, risking damage to both die and the test hardware. Substituting the CRES layer with an alternative material that is highly conductive and inert (non-reactive), such as gold, could prove beneficial. Unlike other metals, gold does not oxidize over time or reoxidize like aluminum layers do.

Solutions

One solution is to change the pad metal structure, but not the aluminum since that would be a critical change in technology. Hundreds of cycle runs and requalification of almost every fab process currently in production would be required. While copper is being used in bond pad metallization, the primary pad metal is still aluminum. Most fabs and processes are not going to switch from aluminum on the bulk of their processes any time too soon. Changing the aluminum metal would essentially shut down the semiconductor industry. However, there are process "enhancements" that can be implemented to eliminate or minimize the corrosion layer. Effectiveness varies by process. In some cases, only a short term gain is realized but that gain might be significant for various operations.

Protecting the Pads

Protecting the aluminum pads with a noble metal, such as gold, would be a benefit. Since gold pads typically have no oxide, CRES goes down significantly (probe tips can still have oxide), probe force is minimize and test yield increases.

One might ask, why not deliver die with the gold layer already on the aluminum pad? Unfortunately, CMOS wafer fab processes don't allow gold to be used in the same facility as silicon. Mixing the two can create bad intermetallics, causing mechanical stress on the silicon that leads to fracturing and chipping (failures) in the die. Since the oxides and corrosion products are not conductive but highly resistive, removal is the process improvement that is sought.

In some instances, aluminum can be ashed to remove oxides with argon plasma or etched with acids/bases to remove the corrosion layers. Layers can also be etched with oxide-only etchants such as BPS100 from Air Products. Ashing is time consuming and can damage the die. Etching with chemicals other than BPS100 can etch too much metal. BPS will etch only the oxide and is a good solution. But even BPS100 is only good for a of couple weeks, since aluminum will regrow its native oxide in time. Once the wafers progress to dicing and are exposed to DI water, other process improvements are required since DI water is a known corrosive agent on aluminum.

The Benefits of ENIG

One other improvement gaining a lot of attention for improving test and assembly yield involves replacing a portion of the aluminum layer using electroless nickel plus immersion gold (ENIG). A number of die suppliers are migrating towards electroless metal finishes on bond pads. Finishes of electroless nickel followed by immersion gold or palladium + immersion gold (ENIG and ENIPIG) improve both test and assembly yields, as well as long-term reliability (**Figure 4**). As part of the electroless processes, the top layers of aluminum, aluminum oxides, and other aluminum corrosion by-products are removed and replaced with strong, chemically bonded, fresh metal layers that are robust and oxide-free.

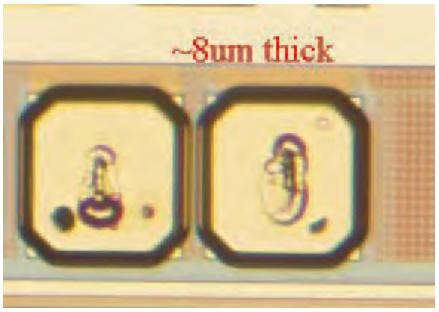

Figure 4. 8µm ENIG on Al pads

Since fabs are unlikely to change the aluminum metal or etch gas, ENIG/ENIPIG provides the best alternatives. Added benefits are not just at test. With the NiAu layer, wirebond is also improved, which increases back-end assembly yield. But electroless processes are not without their drawbacks. One problem with electroless finishes involves shorting of closely spaced bond pads during the plating process.

Wafer Level Test

Earlier we stated the improvement cannot cost more than the time at retest and overall process cost of test or cleaning to improve test. Typically, a wafer probe has a first pass test on all die for opens and shorts. This quick test can provide an expedited pass/fail test without the complete parametric test and associated cycle time. Once the opens/short test is complete, full parametric test is performed. At some point during parametric testing, the probe needles have to be cleaned due to contract resistance (combination of dirty probe needles and wafer CRES). Parametric probing resumes at some interval prior to cyclic cleaning. When the parametric testing is complete, the probe needles are cleaned once again, followed by retest of previously failed open/short units. Those units that pass are then tested for full functionality (parametric). On a 300mm wafer, this cleaning and retest can add up to hours per wafer lot. At hundreds of dollars/hour for test time and thousands of dollars per test card, eliminating corrosion on the bond pad is critical. Also remember that every good die is not recovered. In other words, false failures cause good die to be scrapped. This yield loss can cost companies millions of dollars.

Adding an ENIG process must cost less than retest, the reduction in life of probe cards due to excess cleaning, and the loss in profit of false failures. And it does. ENIG can be as cheap as tens of dollars per wafer. This cost per wafer for ENIG is greatly offset just by the cycle time of cleaning probe cards.

The advantage of ENIG over standard electroplating is that ENIG is a maskless process. Electroless finishes adhere only to the target metals on the die, thus eliminating the time and cost of creating and exposing masks to pattern the deposit. The increasing cost of gold also gives electroless finishes a growing cost over conventional sputtering and plating for typical electrolytic finishes.

The Downside to ENIG

The major problem with electroless finishes, shared with electrolytic plated finishes, is that the deposited layers grow wider at the same rate as they grow higher. The result is a mushroom shape over the target area. Pads with tight pitch will short. This is a limitation for tightly packed bond pads at a time when closer packing is a major goal. The present method to work around this is depositing and curing organic insulators such as polyimide (PI) or polybenzoazole (PBO) prior to electroless processing. The organic insulators, typically 4um thick, provide the isolation and barrier to prevent mushroom shorts during electroless plating. A 2um layer of Ni can then be plated on the bond pads.

The added cycle time and cost of PBO/PI processing almost eliminates the benefits of ENIG processing. PBO/PI materials are not cheap. PBO/PI processing may include up to two addition days of cycle time. PBO and PI also increase mechanical stress, which can lead to electro-mechanical failures, particularly on thinned die. A further drawback is the high processing temperatures required for curing the PBO and PI, approaching 375°C on some materials. The associated stresses as a result of temperatures and polyimide raise concerns for test failures that could mitigate any process improvements.

To avoid those costs and problems, a process replacing the PBO/PI approach, with significant reductions in cycle time and cost is required. A process has been demonstrated up to 10um nickel thickness without bridging to adjacent pads. This process also allows pad size reduction. A NiAu island (**Figure 5**) can be created in the middle of the pad with the aluminum serving as a solder barrier.

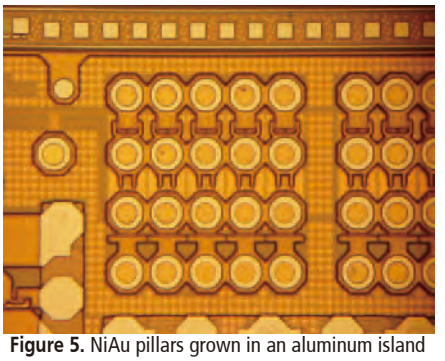

Figure 5. NiAu pillars grown in an aluminum island

Summary

This paper has identified the root cause of bond pad corrosion beginning in the wafer fab. Using fluorine etchants to open windows in the passivation over the aluminum pads leaves residual fluorine in the aluminum matrix. This incorporated fluorine accelerates corrosion and Al(O) growth leading to high contact resistance (CRES). High CRES contributes to poor probing including reprobe/retest, reduces life on probe hardware and false failures of KGD.

As discussed earlier, the fluorine etch will not be eliminated, thus the CRES problem needs to be addressed with other processing. Chemical etching and plasma were introduced as intermediate solutions. To for longer term improvement, ENIG and ENIPIG were introduced as solutions. Electroless processing removes the surface aluminum and its corrosion layers are replaced by a layer of nickel followed by a more robust and noble gold layer. Probing on gold is much more robust, yielding improvements at test and also in the final assembly processing.

To overcome the issue of closely spaced pads there are alternatives to mitigate shorting between the pads. CVInc has identified processed that don't require PI/PBO processing assuring a good cost effective solution with no increases in cycle time for ENIG processing.

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How to Dice Fragile MEMS Devices

By Alissa M. Fitzgerald, Ph.D. and Brent M. Huigens [AMFitzgerald & Associates]

In the world of micro-electromechanical systems [MEMS],silicon wafer processing is used to create micro-mechanical structures that have a wide variety of functions depending on their size and shape. To function as a sensor or actuator, a MEMS device must have a moving part; generally a cantilevered or suspended beam or plate. Microfluidic chips, while structurally robust, have narrow, meandering channels and reservoirs or hidden cavities that must remain free of contaminants. All of these delicate features make MEMS wafers very tricky to dice.

Traditional wafer sawing is a violent, messy process. A high-speed diamond grit wheel makes orthogonal cutting passes on the wafer, while bathed generously with water to keep the wafer and cutting wheel from overheating. The wheel literally grinds its way through the silicon like a more sophisticated version of the mason's tile saw. At the end of the process, the diced wafer is completely covered with a slurry of fine silicon grit which must be washed off.

Engineers have devised clever tricks to protect their MEMS devices during sawing, most of which are manual and don't scale well for volume production. To protect fragile suspended mechanical structures, or to keep grit out of narrow areas (**Figure 1**), engineers might flood the wafer with photoresist or wax to fix the parts temporarily and later dissolve the photoresist in solvents. For wafers with cavities or complex microfluidics that might get clogged with slurry, heat/UV release tapes might be applied to the top of the wafer before dicing to prevent slurry from entering. After dicing, the protective tape must be manually removed from each chip, which can damage fragile features due to residual adhesion and/or high electrostatic forces. Scribe and break is a tecnique that involves scoring the wafer with a diamond scribe and then taking advantage of crystal planes to snap the die apart. Any misalignment of the scribe line with the crystal plane, however, would cause the resulting crack to run through the die and destroy it.

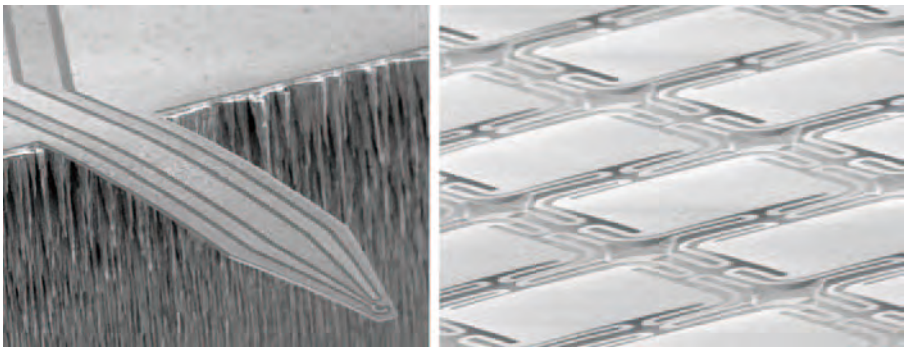

Figure 1. Examples of fragile MEMS structures which can easily be damaged by dicing slurry and grit. Left: A micro-cantilever. Right: Array of electrostatically actuated pixels

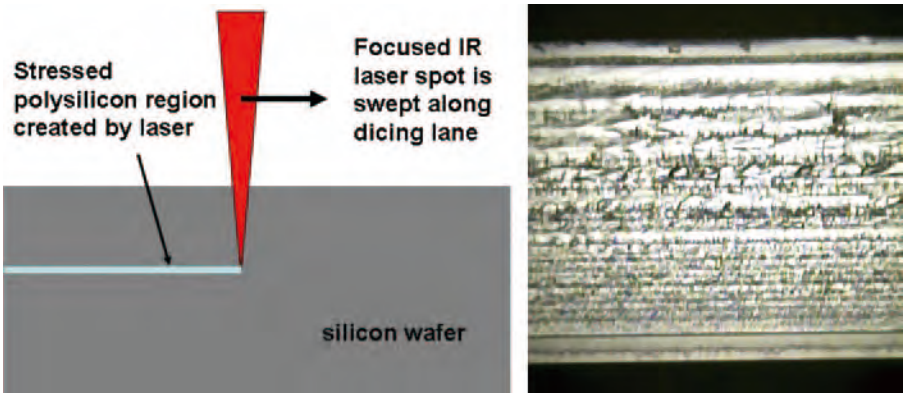

Figure 2. Left: Stealth dicing uses a focused infrared laser beam to locally melt silicon. Right: Micrograph of a chip edge which reveals the multiple laser passes

Engineers have also resorted to using deep reactive ion etch (DRIE) to singulate wafers. Although this is effective, it is an order magnitude more expensive process step. As a last resort, the MEMS device might be designed such that it could be diced while still monolithic, and then a lower-level sacrificial material layer would be etched away post-dicing to release the delicate MEMS structure. In some cases, such a release step can be performed while the wafer is still attached to dicing tape, but for many etch chemistries, the chips must be removed from the tape and processed individually.

Stealth Dicing and How it Works

In the last 7 years, a new technology called "stealth" dicing* has emerged.[1] In stealth dicing, an infrared laser beam is focused to an ~2µm spot within the depth of the silicon wafer and scanned along the dicing lanes. Focused heating from the laser creates highly localized and brief melting, transforming crystal silicon into flawed polycrystalline silicon surrounded by a field of concentrated stress.[2] The laser is sequentially focused at different depths in the wafer, so that a vertical plane of polysilicon is formed in the dicing lane within the thickness of the wafer (**Figure 2**). In striking contrast to traditional laser cutting, where the laser intensely heats the surface of the wafer, burns its way through, and leaves behind slag and rough edges, stealth dicing leaves no visible marks on the wafer's outer surface.

After laser scanning, gentle mechanical tension, created by radially stretching the dicing tape to which the wafer has been mounted, will subsequently cause the silicon wafer to fracture. Because the polysilicon is under stress and substantially weaker than the surrounding crystalline silicon, the wafer separates cleanly along the path that was swept by the laser. Beautifully cleaved die are produced with minimal kerf loss, no grit and no chipping. The tape can be kept in its expanded state so that the die may be easily plucked by machine or by hand.

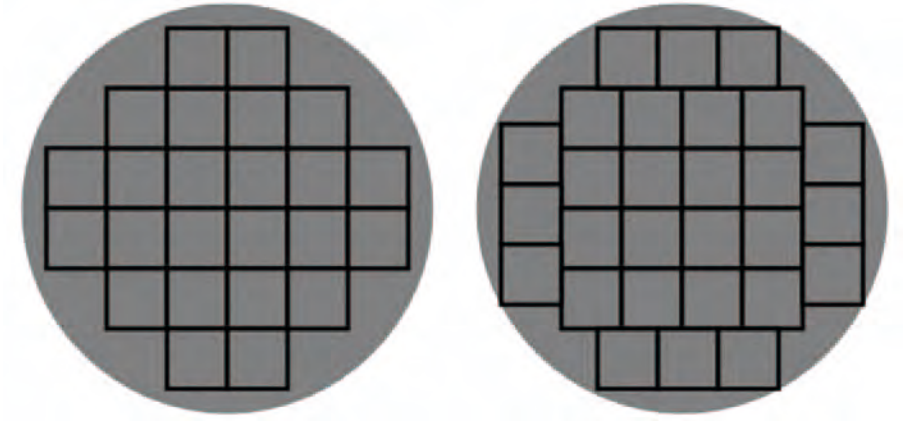

Figure 3. Stealth dicing enables non-Manhattan wafer layouts. Left: Traditional sawing requires alignment of all dicing lanes. Right: Dicing lanes can be staggered to maximize die per wafer

Advantages

Stealth dicing offers significant advantages. The complete elimination of the vibration, liquids and grit associated with traditional sawing is very attractive, if not essential, for dicing of most types of MEMS. But stealth has much to offer any silicon wafer-based technology. Because a laser is used instead of a saw blade, dicing lanes can be shrunk from the typical 100µm down to only 10µm. For wafers with small die, switching to stealth dicing will enable more die per wafer by recovering space once needed for dicing lanes.

Stealth dicing also accommodates complex layouts and unusual die shapes. Traditional sawing is rectilinear, so chips must be in Manhattan grid format. For larger chip sizes, this generally means that not all of the wafer area can be utilized, or if it is, sub-dicing is required. (**Figure 3**) The stealth dicing laser rasters along a pre-programmed path, so offset grid formats are feasible, as well as unusual chip shapes, such as hexagons (**Figure 4**). Finally, because stealth dicing tools are outfitted with infrared optics, it is possible to align the laser path to either a front or a backside wafer pattern. This enables the wafer to be placed face down against the tape and still achieve good alignment.

Limitations

At the moment, stealth dicing may only be used on silicon wafers. The laser path must be transparent to infrared light, so this means that the dicing lanes must be free of oxides, nitrides and any metals. Bonded wafers may not be fully diced by stealth, although hybrid approaches (sawing through a top wafer, followed by stealth) are certainly possible. Dicing lanes must also be relatively smooth, to prevent the laser light from scattering.

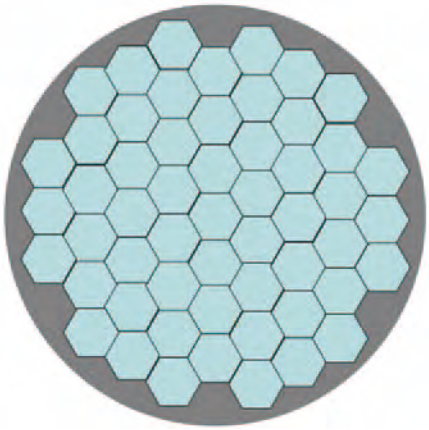

Figure 4. Unusual die shapes are possible with stealth dicing

Costs

As it is a new technology, stealth dicing is more expensive than traditional wafer sawing. Longer set-up time is needed to program the laser path for each dicing pattern and to tune the laser spot for wafer thickness and impurities. Stealth dicing service providers will charge NRE for this setup time, which makes it less economical for small wafer batches.

These added costs should be carefully weighed against factors such as speed, throughput, handling and die yield. In the case of fragile MEMS devices, stealth dicing is almost always worth its extra expense.

Conclusions

Stealth dicing technology eliminates a problematic and yield-killing step for many types of MEMS devices. At our company, we have used stealth dicing to singulate chips of electrostatic actuators, cantilevers, thin membranes and narrow microfluidic channels with great success. Stealth dicing is a superior solution, eliminating the many inefficient and manual tricks that must otherwise be used to safeguard MEMS during traditional wafer sawing. As stealth dicing technology becomes more widely known and utilized, cost will decrease. With time, we fully expect stealth dicing to become the de facto dicing method for fragile MEMS devices.

*a term coined by Hamamatsu Photonics

References

1. F. Fukuyo et al., "Stealth Dicing Technology and Applications", Proceedings of the 6th Symposium on Laser Precision Microfabrication(LPM2005), (2005).
2. E. Ohmura et al., "Internal modified-layer formation mechanism into silicon with nanosecond laser", Journal of Achievements in Materials and Manufacturing Engineering 17, 381(2006).

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Dispensing Advantages for MEMS Wafer Capping

By Akira Morita [Nordson ASYMTEK]

There are many applications for fluid dispensing in MEMS device manufacturing. In MEMS packaging, one area where dispensing plays a significant role is in wafer capping MEMS before dicing.

MEMS are extremely fragile. The slightest touch, vibration, or contamination can damage them. The dicing process is full of obstacles because the flow of water used in dicing and the particulates discharged in the process can destroy or contaminate the MEMS. Therefore, MEMS devices need a protective covering to shield them during the dicing process. Thus, wafer capping is done before dicing.

MEMS wafer capping is a process that has been around for about 10 years. However, back then, most of the MEMS devices were used in applications where the package had to be hermetically sealed and extremely reliable. The process was quite costly, so wafer capping wasn't a common practice. Today, MEMS are used in consumer products like microphones in mobile phones and the mouse for PCs. Since these new applications do not require MEMS to be hermetically sealed, new manufacturing methods and challenges have arisen. One of these new methods is dispensing the sealant and adhesives in the wafer capping process. Jet dispensing systems have been designed to specifically handle MEMS wafer capping.

The Wafer Capping Process

The package structure for MEMS wafer capping consists of a substrate, a wafer with MEMS, and a glass wafer (or another silicon wafer) containing the cavities that cap the MEMS. Die-attach adhesive, such as silver epoxy, is dispensed in thin horizontal and vertical lines onto a film-frame wafer to attach the MEMS devices. A layer of sealant is jetted around the rim of each cavity on the glass wafer. The sealant can be a UV cure adhesive, low-temperature solder, covalent, or a glass frit. The MEMS structure is then capped with the glass wafer. A UV light penetrates the glass wafer to cure the adhesive. The wafer is then diced. The cap keeps the MEMS protected during the wafer dicing process.

The equipment used in MEMS wafer capping is a dispensing work cell that consists of an automated fluid dispensing system integrated with a same-side film-frame loader/unloader. This single work cell minimizes the footprint and maximizes throughput. The system is fully enclosed with interlocked doors and windows (**Figure 1**).

MEMS are 1 to 100µm in size, and MEMS devices generally range in size from 20µm to 1mm. The volumes of fluid dispensed must be at the micron level and dispensed precisely in very thin lines. The corners must be extremely defined so each cavity section covers the MEMS, ensures the MEMS device is well seated, and the glass connects properly to the wafer. Volumetric control must be maintained to ensure fluid deposition is accurate and within tight tolerances. Many of the end products that contain these devices

Figure 1. Integrated workcell with a loader and dispenser for MEMS wafer capping

Figure 2. Dispensing onto a wafer

are manufactured in large volumes, so wafer handlers, automated fluid dispensers, and the software that drives them must automatically monitor and control fluid viscosity, dispense weight, pressure, line widths, and placement at the speed required to achieve desired throughput while maintaining high yields. Reduction of manufacturing costs is also important because packaging is a determining factor for the production cost of MEMS (**Figure 2**).

Jet Dispensing for Wafer Capping

In addition to all the advantages inherent in jet dispensing technology, there are three distinct advantages for MEMS wafer capping:

- speed
- the ability to dispense fine lines and sharp corners
- elimination of the knit line or "dog-bone" effect

The precision, accuracy, and speed that jetting provides meshes well with MEMS requirements. Jetting is the process where fluid is rapidly ejected through a nozzle, using the fluid momentum to break free from the nozzle. A discrete, controlled volume of material is ejected with each jetting cycle. Jetting is fast because when moving from one dispense location to the next, it is not necessary to move up and down in the Z-axis. Dispense speeds ranging from 20mm-70mm/sec for MEMS applications, depending on the fluid and application requirements, offer higher throughput than needle

dispensing. For example, in a typical application, a jet can dispense at 80mm/sec as compared to 30mm/sec with a needle. Because jetting is a non-contact process, it is less sensitive to the dispense gap for "potato chip" wafer topology of wafers that aren't perfectly flat.

Jet valves can dispense dots to form line widths as narrow as 300 or 400µm (**Figure 3**). Innovations like calibrated process jetting (CPJ) significantly reduce process variability. Pressure is adjusted to maintain constant mass per dot and proprietary software and hardware automatically compensate the dispensing process for both fluid viscosity changes over time and batch-to-batch variations. These factors are especially important for working with MEMS as CPJ increases dispense accuracy, delivers higher yields, and ensures consistent Takt time (pace set for industrial manufacturing lines) for improved process capability, resulting in a highly repeatable process. Set-up to set-up and line-to-line variations are minimized and the need for operator interaction eliminated. Jetting is faster and makes better lines and sharper corners than other technologies.

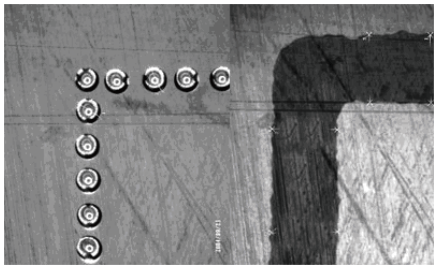

Figure 3. DispenseJet® valve jets dots to form 400µm lines

A significant concern in dispensing is the knit line — the beginning and end-point of the dispensed line. There needs to be a seamless connection and the line width must not vary. For example, if too much material is dispensed at the beginning or end of the line, or the end doesn't break cleanly, the result is referred to as the "dog-bone effect," because the extra fluid at the ends of the line resemble a dog bone. This often happens with needle dispensing due to excess fluid left when the needle is retracted. In contrast, a jet dispenser shears the material, eliminating the dog-bone effect and providing a seamless connection.

Other MEMS Dispensing and Jetting Applications

In addition to wafer capping, jetting is used in many other MEMS manufacturing applications. For example,jetting silicone isolates the MEMS chip from the environment by encapsulating the wire bonds. MEMS packages on flex printed circuit board require underfill for the CMOS image processor of a camera module assembly. Jet dispensing is an ideal way to deliver that underfill. Finally, the SmartPhone alone has at least 15 parts that utilize MEMS where automated fluid dispensing is required.

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LED Dicing: The Sapphire Blaze Indeed

By Jeffrey Albelo [Quantum-Group Consulting, Ltd.]

Rubies are red and sapphires are blue and it's all because of 10dq. With the notable exception of emeralds, most gemstones are based on transition metal impurities suspended in a crystalline corundum (Al_2O_3) matrix. 10dq, or more formally, Δ10dq, which refers to the energy gap imposed upon formerly degenerate energy levels (**Figure 1**) by the presence of ligands (moieties coordinated to transition metal ions in inorganic and organometallic complexes). It is the oxygen atoms

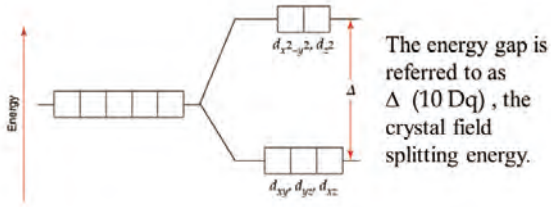

Figure 1. A conceptual representation of crystal field splitting

or Ti_4+ and Fe_2+ as a charge transfer pair in sapphires, that account for the crystal field splitting exhibited in these gemstones and thence their characteristic colors.

The size of this splitting determines the absorption wavelength upon excitation by visible light and is analogous to the band gap in LED and other similarly conceived devices. The larger the gap the more energetic the photon ($h\nu \geq \Delta 10dq$) must be to promote electrons from the lower energy orbitals to the higher. More practically, the size of Δ10qd is directly proportional to the observed color of the crystal; ruby (red) for instance, has a larger gap than its sapphire counterpart (blue). Put another way, the increase in the energy gap between d-orbitals causes the absorption of higher energy photons and a corresponding red shift for the observed or transmitted color, since the observed or transmitted color is the complementary color of the absorbed wavelength. Somewhere between really boring and pretty colors, the LED industry exists. Band-gap-engineered, multilayer junctions sitting atop very clean sapphire make for an interesting juxtaposition between Mother Nature and human efforts. Mother Nature creates value by making her sapphire dirty. Human-kind takes great pains to keep its sapphire squeaky clean and highly refined to create value on LED, (Si on Sapphire (SOS) for RF devices where analog and digital processing can be handled on a single monolith), or other hybrid applications. In terms of value creation, Mother Nature wins, with about $30B in annual gem sales compared with the combined engineered sapphire market at around $16B. Take heart, even though she who must be obeyed has been at it for an age we win in the end, with the advent of green lighting solutions coming on the heels of government mandates for same, the five year CAGR >20% far outstrips projected gem sales growth by nearly 2:1.

Once formed, using whichever process, (please ignore that "lift-off" noise from behind the curtain) these devices must be singulated. At last count, there were three commercially viable choices for affecting singulation: mechanical scribe-and-break, laser scribe-and-break, and laser full-cut; or in other words "slow, slower, and slowest" depending upon one's perspective. At present, there is not a solution to address the cost-of-ownership (CoO) equation in an ideal manner. Particular attention, from a dicing solution perspective, has been paid to the three yield categories depicted in **Figure 2**, all of which are affected by all of the commercially available dicing solutions. There is yet another possibility. Evidence shows that rapid bulk etching of alumina may be economically feasible. The etch solutions presently being deployed are

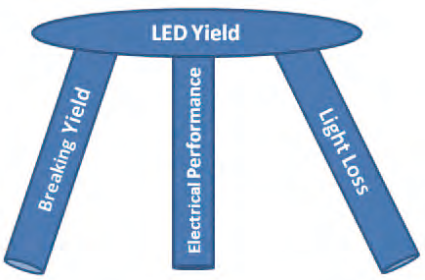

Figure 2. LED yield considerations, the 3-legged piano stool, very stable, but each leg is equivalently important in delivering stability.

aimed at LED packaging applications, an area where laser-based products have yet to make a showing. One might even imagine solutions where etch-based singulation might be considered, but it is not yet commercially available.

Laser-based scribing

Although advances in mechanical scribing have been deployed, the industry has shifted to laser-based processes. This shift has been dictated by the need to raise LED yields to improve the distribution between the two basic (somewhat tongue-in-cheek) LED categories: high-quality LEDs and Christmas lights. The issue associated with laser-based processes is the damage induced by the laser beam, as it is invariably focused either onto the surface or into the bulk via very high NA lenses. The problem with this laser approach is the inherent limitations imposed by basic physics that serve to bind the ultimate throughput and damage performance. Tamhankar and Patel presented data at 2010's ICALEO suggesting limitations encountered in ns processes, **Figure 3**, where increasing fluence showed diminishing returns in scribe depth.

Although their proposed solution involved splitting the laser beams to increase throughput, the scribe depth was limited to ~50µm, which still requires reasonably high breaking force, generates debris, and causes

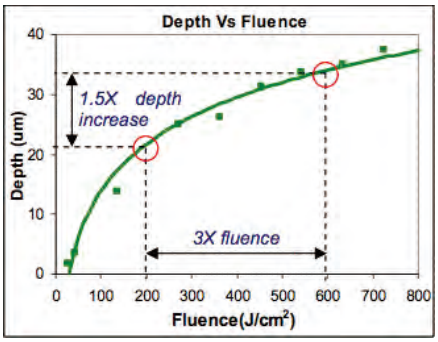

Figure 3. Diminishing returns. Hitting the sapphire harder ultimately yields scribes of unremarkable depth and induces loss in quantum efficiency and breaking yield. (Image courtesy of Spectra-Physics)

crystal damage. The experienced in the audience are thinking, this limitation is imposed by pulse width; a correct, but ultimately incomplete answer.

The present bestiary contains commercial solutions using picosecond lasers that fare better in terms of light loss, but struggle with Distributed Bragg Reflector (DBR) layers, CoO, or are ultimately limited by the breaking yield by virtue of the applied force required to affect singulation. To improve yield and quality, one must reduce the force required to free these dice from their mother substrate. This means a laser process must be created that enhances the defect formed in the sapphire, without requiring more time, impeding the electrical performance, or optically damaging the substrate.

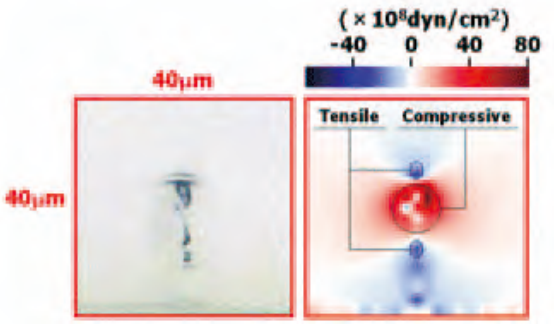

Figure 4. Stressed out. Side (L) and top-down view of the Stealth defects in Si. Stress in the crystal is a result of deposited energy which distorted the crystal and is a result of exceeding the optical breakdown threshold in the material, which even when induced by short pulses, still creates thermal damage. (Image courtesy of Disco)

Stealth dicing

By now everyone (even that guy in the desert with the coke bottle that fell from the sky in The God's Must be Crazy) has heard about stealth dicing and opinions are as common as post-dicing defects. Fans and detractors alike will agree the process takes too long and still has legions of casualties as a result of post singulation failures in one (only one?) of the three aforementioned quality areas. The reasons for this are related to deposited energy, even with short pulses, the joules dropped onto the surface or into the bulk ultimately end up somewhere. If one must employ a process that requires multiple passes, the advantage of the short pulse laser is somewhat negated as the crystal still "feels" somewhat roughly handled. To wit, even Disco reports there is a stress field associated with the stealth defect (read: Optical Breakdown, OB) delivered into single crystal material.

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Although **Figure 4** is for silicon, the concept is a well-placed coffin nail for sapphire, in that the surface faces of the dice will bear the morphology associated with the stress field so-created. In addition to, or perhaps because of this stress, the surface faces are rough and non-uniform, resulting in electrical performance issues associated with increased operating temperature. This increase in temperature is a result (among other factors) of reflected light into the device.

Why, one might ask, does the crystal care if the defect is formed neatly beneath the surface? The mechanism of formation requires exceeding the optical breakdown threshold of the material, and herein lies the problem with the bigger hammer approach. Silicon substrates lend themselves to optically induced damage because, within limitations, the final performance of the device being singulated is not affected by the optical quality of the edge (micro-cracking notwithstanding). For LEDs, the situation is quite different. **Figure 5** portrays the evolution of light from the device as a mathematical model of intensity vs. position; a fair amount of light passes into and through the substrate. If the light has difficulty escaping, the substrate temperature rises. The junction efficiency decreases with rising temperature, so the extracted light fraction per watt of electrical energy falls. This takes the devices in the opposite direction of all the cap-ex to date, where even small efficiency gains were pursued with abandon.

At this juncture, it is useful to call to mind that deposited laser energy is transferred to the lattice as electronic interactions and as heat via collisions with phonons. Both processes, for very short pulses, can be temporarily decoupled since the main energy transfer occurs via the hot electron sink after the pulse has stopped. For pulses longer than a few tens of picoseconds, the mechanism involves heating conduction-band electrons by the laser pulse and transferring this energy to the lattice in a photon-electron-phonon interaction. Damage occurs by a conventional heat deposition process resulting in a phase transformation of the dielectric material. To achieve OB (the stealth defect) the material has to be transformed into an absorber by having its electrons "pumped" by subsequent laser pulses to the point of so-called avalanche onset, where free electrons are created and dielectric breakdown occurs. Without breaking into a full derivation ('Meet the Fokker-Plank equation' leaps to mind), the reader must accept on face value that the OB phenomenon is bounded by a critical fluence, F*cr*, which is directly proportional to the natural log of the

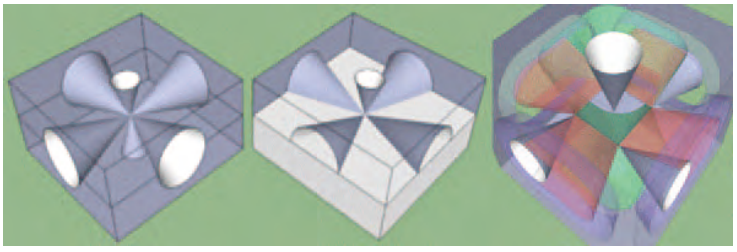

Figure 5. Snow Cones. Despite marketing efforts to the contrary, physics requires all processes to play by the same set of rules. From L to R, the simplified light cone model, the interaction with the sapphire substrate and finally, the fully populated light evolution model, illustrating the complexity of extracting light from these devices and the volume of light traveling into and through the sapphire.

population inversion (from a number density point of view) caused by multi-photon processes.

$$F_{cr} = I_0 \tau \frac{1}{2}\left(\frac{\pi}{\ln 2}\right)^{\frac{1}{2}}$$

Therefore, this threshold fluence falls as the pulse width decreases, so the astute reader solves the present problem by simply applying a femtosecond laser to the issue of LED singulation, figuring that lower delivered fluence will yield less substrate damage. A correct observation, but again, at its core, it is an incomplete answer.

A novel approach

While collateral damage can be reduced by judicious choice of pulse width, the act of singulation still requires perturbation of the lattice and that requires some minimum amount of damage. In order for the yield to remain commercially acceptable, the amount of force applied "to break" must fall below some upper limit, imposed by, among other things, substrate thickness. Exceeding this limit will produce an unacceptable level of device failures and/or broken pieces. Keeping extracted quantum efficiency firmly in mind, one is left to conclude that there is a maximum yield for this process, above which one cannot aspire, unless a novel approach is contemplated.

Most of the LED devices presently produced are either singulated using a plain vanilla ablative technique to affect surface scribes or an OB technique (Stealth, et al.) relying on internal breakdown of the dielectric from very tightly focused beams. Both approaches create device failures, via one or more well-known and oft lamented mechanisms. A novel approach might employ a closely related phenomenon known as filamentation. Studied extensively back in the 1970s, Marburger, et al, discussed the formation of filaments in air. A condensed matter model and experimental was not undertaken until much later, and has only recently become commercially interesting as the advent of reliable and affordable short pulse lasers has

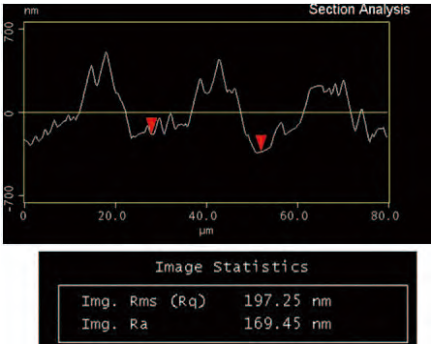

Figure 6. A not so winding road. AFM roughness of the Sapphire substrate following singulation using the proposed filamentation technique. Note the RMS roughness is < 200 nm. This roughness is adjustable over a range that makes it perfectly feasible to program the dice edges to deliver optimal light transmission, thereby solving one mode of LED yield loss, while also addressing the other two post singulation yield issues.

come to pass. This P*cr*, is given by,

$$F_{cr} = \pi\left(\frac{d}{2}\right)^2 I = \frac{\pi(0.61)^2\lambda^2}{8n_0 n_2}$$

where n0 and n2 are the linear and nonlinear refractive indices of the material. Filamentation occurs due to self-focusing that transpires under these power conditions and is balanced against defocusing that occurs as a result of the weak plasma formed by the multi-photon processes, which should sound familiar from the previous discussion of OB. Depending on fluence, these transients can form and persist for many 10's of meters in air. Their condensed matter cousins can similarly persist for millimeters in transparent media. Upon choosing the proper conditions, one can envision a process where the damage problem is eliminated by formation of plasma dense enough to vaporize a gossamer thin tube of material; it can be accomplished at a previously unheard of rate and as a bonus it can eliminate the reflection problems associated with traditional methods.

It is this latter piece that bears minor exposition. In the same fashion that a Ronchi grating operates to enhance light passage across a barrier, one can, using this new technique, match the wavelength of the device with the spacing of the edge roughness. As **Figure 6** shows, die-edge roughness can be controlled by judicious choice of process conditions and therefore

Figure 7. Where angels tremble while they gaze. The edge view of 100µm sapphire singulated with the proposed filamentation approach. The visible edge has been scribed and diced, visible on either side, is the modified regions wherein the defect has been created by plasma induced ablation of the material.

can deliver LEDs of higher quantum efficiency simply by virtue of their singulation. As it turns out, this approach is adjustable, over a range from <200nm up to 1000nm in RMS edge roughness by simply choosing the appropriate condition.

Conclusion

In all the ways the LED singulation process can go awry, this approach creates a finished product, a singulated die that is superior to conventional dicing methodology. It bears investigating this phenomenon more fully, as there is ample commercial impetus to do so. **Figure 7** is an edge view of sapphire singulated at 600mm/sec. where the defect persists from top surface to bottom surface, through the substrate's 100µm thickness. This defect is clearly visible as it extends throughout the bulk of the sapphire.

Figure 7 is an edge view of sapphire singulated at 600mm/sec where the defect persists from top surface to bottom surface, through the substrate's 100µm thickness. This defect, so rendered, is clearly visible as it extends throughout the bulk of the sapphire.

Thomas Gray, English Poet and Professor at Cambridge (1716-1771) once wrote, "… the living throne, the sapphire-blaze, where angels tremble while they gaze, he saw, but blasted with excess of light, closed his eyes in endless night." It is likely this is not to be, in that there exists a solution to deliver the "excess of light". One need only seek a suitable commercialization route to realize its advantages.

Jeffrey Albelo, president and CEO Quantum-Group Consulting, Ltd., may be contacted at albeloj@qcsgroup.com.

(continued from Page 13)

Session 2 – 3D Process Advancements Part I, Session 4 – Fan-Out Wafer Level Packaging Technologies and Session 8 – 3D Process Advancements Part II.

Figure 8. Peter Ramm, Fraunhofer EMFT, introduces plenary speaker, Matt Nowak Qualcomm.

Stimulating Plenary Sessions

Prior to each day's technical sessions, attendees were treated to a stimulating morning plenary speech. The first was "High Density TSV Chip Stacking: Fabless Infrastructure Status" by Matt Nowak of Qualcomm. He presented some examples of several chip stacking partitions that are reportedly in development for productization, and discussed the progress made with respect to previously perceived challenges. Mr. Nowak went on to say, "Especially critical for the productization of high density TSV technology for high volume mobile wireless applications will be the readiness of the fabless supply chain infrastructure, including industry standards, supply chain business models for stacked memory cubes, and competitive pricing."

The second plenary talk was "Evolution, Challenge and Outlook of 3D Si/IC Integrations" by John Lau, Ph.D., of ITRI. He explained the difference between 3D IC packaging and 3D IC or Si integration

Figure 9. Vern Solberg of Invensas, is among a full house tuned in to John Lau's plenary talk

was that integration incorporates through silicon vias (TSVs). Dr. Lau covered the origin and evolution of 3D integration, technology development roadmaps, and he proposed a few generic, low-cost, and thermally-enhanced 3D IC integration System-in-Packages (SiPs) with various passive TSV interposers for small form factor, high performance, low power and wide bandwidth applications.

Lively Panel Discussions

Figure 10. An unidentified attendee queries the infrastructure panel, which was moderated by Simon McElrea, Invensas

This year's IWLPC program included two panel discussions that provoked quite a few questions and debate among the panelists. "3D Infrastructure Issues for Technology Adoption", moderated by Simon McElrea of Invensas Corp. brought together a distinguished panel consisting of Sesh Ramaswami, Ron Leckie, Peter Ramm, Ph.D., Andre Rouzaud, Ph.D., Jan Vardaman, and Jim Walker.

"Will 2.5D and 3D Compete or Coexist?" was the title of the second discussion with panelists Scott Jewler, Ron Huemoeller, Phil Marcoux and Rao Tummala, Ph.D., moderated by Francoise von Trapp of 3D InCites. Each panelist made a short presentation and stated their case before the floor was opened for questions The consensus opinion favored coexistence of 2.5D and 3D integration.

Entertaining Keynote

Following Wednesday night's dinner, Raj Master, General Manager for IC Packaging, Silicon Operations, Quality and Reliability for all hardware products at Microsoft gave an entertaining keynote speech titled "Thermal and Power Considerations in Consumer Electronics." He kept the audience laughing

Figure 11. The 3D Panel discussed 2.5D vs. 3D technologies. (L-R) Phil Marcoux, consultant, PPM ; Ron Huemoeller, Amkor ; Scott Jewler, Powertech Technologies ; Rao Tummala, Georgia Tech's 3D PRC ; and moderator, Francoise von Trapp

with timely jokes, amusing examples, and funny illustrations while describing the very serious thermal management challenges facing 3D IC packaging and integration as computing products strive to operate faster and shrink in size. Thermal management can no longer be addressed solely at the system level using heat sinks and fans inside the product enclosure. Heat must be dissipated at the device level and must be capable of withstanding shock, drop impact, and bending often encountered by portable products.

Figure 12. Raj Master, General Manager for IC Packaging, Silicon Operations, Quality and Reliability for all hardware products at Microsoft entertains the dinner crowd with his keynote speech titled "Thermal and Power Considerations in Consumer Electronics."

For the first time this year, IWLPC provided video coverage of some of the plenary talks, keynotes, and platinum sponsors. Clips can be viewed at www.iwlpc.com and www.chipscalereview.com.

Save the Date

IWLPC 2012 will have an expanded exhibition hall when it moves to the Doubletree Hotel in San Jose, CA on November 5 – 8, 2012. Many of today's WLP challenges will be addressed in the coming year. Don't miss next year's event to learn about all the progress.

Nordson Corporation Establishes Steve Adamson Memorial Annual Scholarship Fund

Steve Adamson, former Nordson ASYMTEK marketing specialist and electronics industry mentor, passed away October 28, 2011, after a 15-month battle with cancer. Nordson ASYMTEK honors his life by funding a $3,000 annual scholarship in Adamson's name with the IMAPS Educational Foundation, whose role is to support student activities related to the study of microelectronic packaging, interconnect and assembly.

"This donation supports the mission of the educational fund, which Steve was instrumental in establishing. We are glad we can honor the memory of Steve in this way," said Michael O'Donoghue, Executive Director IMAPS.

Adamson started with Nordson ASYMTEK in 1998 as applications lab manager, and most recently was market development manager for the semiconductor packaging and hard disk drive industries. Over his career with Nordson ASYMTEK, Adamson contributed to the success of several important projects, including the Axiom and DispenseJet product lines. Adamson previously held positions with Kodak, Motorola in the U.S., and Plessey, International Computers Ltd in the U.K. He was awarded five US and two UK patents. Originally from the UK, he held a Higher National Certificate in Electrical Engineering from Stockport College of Technology. In 2005 he was presented an award by the San Diego Engineering Council for "Outstanding Service to Electrical Engineering".

"We will miss Steve's creativity, intellectual curiosity, and friendship. And the industry will miss his active participation and leadership," stated Greg Hartmeier, vice president, Nordson ASYMTEK.

Adamson was very active in the International Microelectronics And Packaging Society (IMAPS), serving as President in 2008 and as chairman of the IMAPS Microelectronic Foundation in 2009. In 2010, he received the IMAPS President's Award in recognition to his lifelong efforts for the organization. Most recently, in early October 2011, he was awarded the Daniel C. Hughes, Jr. Memorial Award by IMAPS, which is presented to the individual who has made the greatest contribution to IMAPS and the microelectronics packaging industry, including technical and/or service contributions. Donations to the fund in his honor can be made at: www.microelectronicsfoundation.org.

Deca Technologies: Changing Packaging by 10x

By Francoise von Trapp, Sr. Technical Editor

At an exclusive launch party held at the home and vineyard of Cypress CEO, T.J. Rodgers, the story unfolded about Deca Technologies, a disruptive packaging start-up backed by Cypress and its solar child, SunPower. Francoise von Trapp, Sr. Technical Editor, was there to tell the tale.

November 9, 2011 just might go down in semiconductor history as the date the whole game changed for semiconductor assembly, packaging and test. This day marked the official launch of Deca Technologies, an interconnect technologies company that intends to offer a novel approach to manufacturing processes for wafer level packaging, based not on semiconductor manufacturing but the solar cell manufacturing processes introduced by SunPower Technologies. In an ironic twist, where SunPower had leveraged the semiconductor manufacturing knowhow of its benefactor company, Cypress Semiconductors, to reduce the cost of manufacturing its solar cells; now the semiconductor packaging industry stands to benefit from knowledge based in solar cell manufacturing.

The story began in 2009 with a conversation and a compelling concept. According to Deca CEO and founder, Tim Olson, the idea blossomed out of the unresolved industry need for solutions that address cycle time, cost of ownership, and process flexibility. The inspiration came by example from SunPower, which, according to SunPower CEO Tom Werner, had developed a low cost way to manufacture high-efficiency silicon solar cells in high volume thanks to lessons learned from Cypress. Olson recognized that these proprietary processes could be adapted to re-engineer core processes for wafer level chip scale packaging (WLCSP). Additionally, as a member of Cypress Semiconductor's technical advisory board, Olson had witnessed the company's ability to breathe life back into SunPower, turning it from a company on the brink of collapse in 2003 to one that reported revenue of $2.2B in 2010. So he approached TJ Rodgers, CEO of Cypress, with the idea. With $35M in seed money from Cypress, work got underway.

Cypress Involvement

Cypress CEO, TJ Rodgers, has vision and likes to take risks. An engineer with degrees in chemistry and physics, he's always looking for a better way to do things. When he's not running Cypress, he's on a quest to produce "the best Pinot Noir in the 'New World." He's done a careful and thorough study of French winemaking processes, and has simulated conditions and processes from France to produce a high-end wine at his winery, Clos de la Tech, in Woodside CA. He's a purist in winemaking; the grapes are foot crushed and never come into contact with machinery (**Figure 1**). The only nod to technology is his custom-designed fermentation controller system from Cypress, where he puts Cypress engineers to work creating systems to gather and analyze data from the tanks, using RF devices to transmit the data to a computer. No expense is spared in this endeavor. "How do you make a small fortune in the wine industry?" Rodgers queried, "Start with a large fortune."

Figure 1. TJ Rodgers explains wine making to the Press.

But where Rodger's is willing to take a loss for the sake of the wine, he's not willing to take a loss for the sake of technology improvements. For example, he abandoned a project on solid state lighting when he realized that the end product couldn't compete with standard lighting on asking selling price (ASP). That's why Cypress invested in SunPower, because he saw opportunity to improve manufacturing processes to reduce the cost of a wafer from $1000/wafer to $10/wafer. Transferring that technology knowledge to Deca Technologies for WLCSP, Rodgers is looking beyond the initial product offering of the WLCSP to the next product on the drawing board; silicon substrates, which up until now have been too costly to become mainstream. "If you can make a wafer for $10, then you can make silicon interconnects that you can put chips on," notes Rodgers, adding that it's about making something both cheaper and better. While WLCSPs are a better performing technology than wire bonded packages, they are more expensive to make. But Deca's technology takes the cost out, reportedly achieving a cheaper WLCSP while retaining high performance.

Deca's Secret Sauce

Deca's success depends on a careful blend of unique manufacturing based on SunPower's continuous wafer flow line rather than a batch process approach; and custom proprietary equipment from suppliers outside the traditional semiconductor equipment manufacturing realm. It's WLCSP process is nearly parallel to SunPower's solar cell back-end of line (BEOL) processes. "We have special stuff that nobody in the world has because of SunPower," notes Olson, adding that exclusivity with suppliers is the key. He said that getting suppliers to agree to exclusivity agreements was a daunting task, but in the end, they were able to accomplish just that, with some agreements for an indefinite amount of

time, and others that are for a minimum of five years. Additionally, the company is hyper-careful with its trade secrets, requiring extreme sensitivity throughout its workforce and restricting access to the manufacturing lines. Olson also said that they have highly educated technicians running the processes at the facility, located within SunPower's complex in the Philippines. "All our manufacturing technologists are English-speaking, degree-level engineers," he said.

Deca's technology spans interconnect levels from chip to package to system, noted Olson, and offer exponential improvements in speed, cost and flexibility. Its first products are in the WLCSP family (**Figures 2**).

Figure 2. Deca's first product is a fan-in WLCSP available in three different configurations

Acknowledging that these are "me too" products, Olson explained that the company's strategy is to enter the market with existing products that are manufactured in breakthrough cycle time; at the lowest total cost of ownership; and can be taken from design to manufacturing in minutes rather than days. This path is the quickest to a solid revenue stream. Next on Deca's roadmap is the technology that has Rodgers all excited: silicon substrates that could provide the cost improved solution for silicon interposer technology.

Ready out of the Gate

With its eye keenly on the analog power management and RF connectivity markets, Deca is ready to roll. "This is not just an idea," noted Olson. "We are ready to go to production." He claims the company achieved 97% yield on the first wafer that went through the line. Now they're achieving above 99% yield. They are fully staffed for one shift and by Q2 2012 anticipate 24/7 operation.

At the time of the launch, Deca has engaged six customers, five of whom report in excess of $1B revenue/year. Olson said the first customer is qualified for production; the next three are undergoing qualification. He anticipates two remaining customers to begin qualification within 90 days. The company expects a significant production ramp by Q4 2012. "2013 will be our first big year," says Olson. This will undoubtedly be an exciting company to watch.

PRODUCT SHOWCASE

ACT IV

By Ron Edgar [Chip Scale Review Contributing Editor]

"Double, double, toil and trouble; Fire burn; and cauldron bubble." To many, the "magic" of the science behind, and the manufacturing of, state-of-the-art electronic devices might as well be the witches' brew from Macbeth. Exotic materials, exacting requirements, all cooked up for a special purpose. I've been revisiting NIST (National Institute of Standards and Technology) to see what they have been doing recently that is of interest to us.

"Fillet of a Fenny snake, in the cauldron boil and bake" . . . Carbon nanotubes show great promise as a possible replacement for copper interconnects on ICs. "But—not so fast." says an article in NIST Tech Beat, August 16, 2011. "Recent tests at the National Institute of Standards and Technology (NIST) suggest device reliability is a major issue." NIST have been studying how carbon nanotubes might behave in real electronic devices and have been focusing on how they interact with metal structures and various kinds of nanotubes structures. In a paper presented at IEEE Nano 2011, Portland, Ore., Aug. 17, 2011, by M.C. Strus, R.R. Keller and N. Barbosa III, Electrical reliability and breakdown mechanisms in single-walled carbon nanotubes, experiments with carbon nanotubes interconnecting metal electrodes showed degradation of the nanotubes interconnect and failure of the metal electrodes. "The common link is that we really need to study the interfaces," says Mark Strus, a NIST postdoctoral researcher. In other experiments with nanotubes networks, where electrons "hop" between nanotubes, failures were seen between nanotubes. Monitoring this provides a means of assessing the reliability of a network. So where do we go from here? " . . . carbon nanotube networks may not be the replacement for copper in logic or memory devices, but they may turn out to be interconnects for flexible electronic displays or photovoltaics," Strus says.

"Eye of newt, and toe of frog, Wool of bat, and tongue of dog" . . . Atomic Force Microscopy (AFM) is a favored method of measurement at the nanoscale but "most can only produce qualitative images. In contrast, contact-resonance force microscopy (CR-FM) enables quantitative mechanical-property mapping. CR-FM involves vibrating the AFM cantilever while its tip is in contact with a sample. In this way, the resonant modes of the cantilever—the "contact resonances"—are excited. From measurements of the contact-resonance frequencies, information is obtained about the interaction forces between the tip and the sample (e.g., contact stiffness). Models for the tip-sample contact mechanics are then used to relate the contact stiffness to mechanical properties such as elastic modulus." Donna Hurley and her team have the goal "to provide tools for nanotechnology research and development that rapidly and nondestructively map the nanoscale mechanical properties of new materials and devices. Measuring localized variations in properties not only yields valuable information on material homogeneity and manufacturability, but also enables early identification of subsurface defects. Our methods also provide size-appropriate data critical for the predictive modeling of device reliability and performance."

"Adder's fork, and blind-worm's sting, lizard's leg and owlet's wing". . . NIST's Engineering Laboratory has recently inaugurated a new Sustainable Manufacturing Program. This is a collaboration between a number of major manufacturers and several universities. Why NIST? In their own words, "This program is aligned with the Engineering Laboratory (EL) mission to promote U.S. innovation and industrial competitiveness in areas of critical national priority." Recent studies conducted by Harvard Business School and the MIT Sloan School of Management concluded that sustainable product and process development across all industry sectors "is essential to remaining competitive." Current efforts have, at best, been sporadic and specific to the organizations who were trying to implement such ideas. With NIST's involvement and the effort of the contributors it is hoped to create innovative methods that can be applied industry-wide in the hope of reducing energy costs, improving processes, encouraging cooperation, and increasing profitability.

"For a charm of powerful trouble, like a hell-broth boil and bubble" . . . Semiconductor research is a vast area and a hard one to keep up with. In an agreement between NIST and AIP (American Institute of Physics), a great deal of research information is now available free of charge. David Seiler of NIST says the available materials "represent research and overviews of critical topics collected from worldwide experts in the field of semiconductor characterization and metrology."

So be sure to visit www.nist.gov regularly as they are a source of invaluable information. And here's wishing us all a happy and prosperous 2012.

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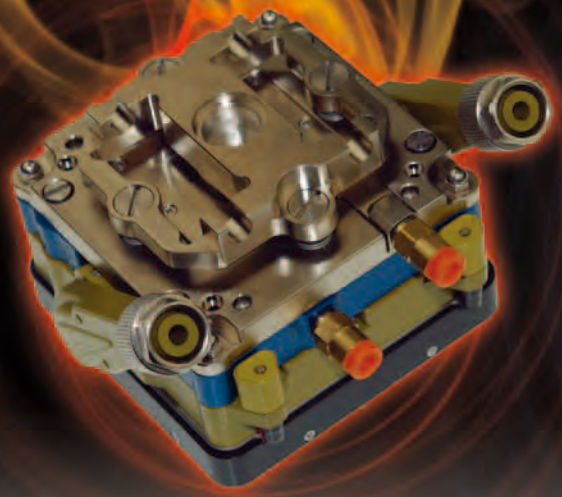

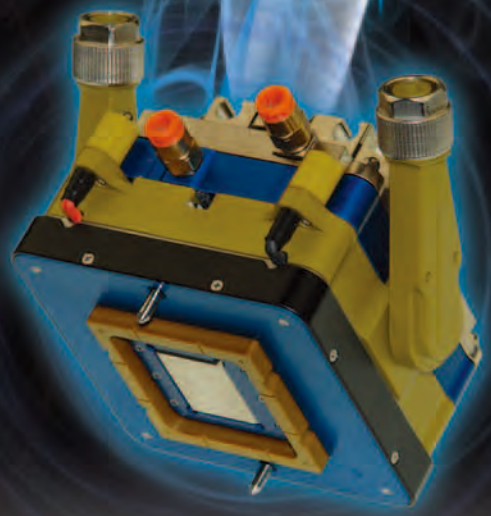

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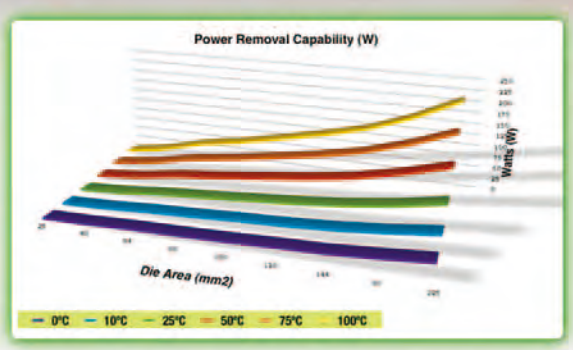

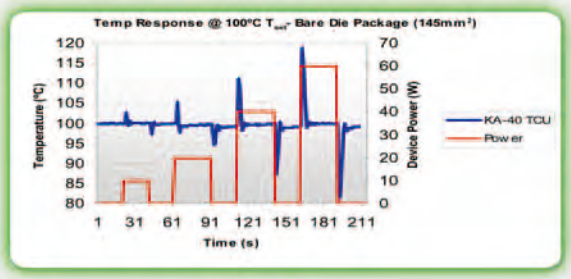

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